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AN-6753

FAN6753 — Highly Integrated Green-Mode PWM Controller

Abstract

This application note describes a detailed design strategy for a high-efficiency compact flyback converter. Design considerations, mathematical equations, and guidelines for a Printed-Circuit-Board (PCB) layout are presented.

Features

- High-Voltage Startup
- Low Operating Current: 2.7mA
- Linearly Decreasing PWM Frequency to 22KHz
- Frequency Hopping to Reduce EMI Emission
- Fixed PWM Frequency: 65KHz
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking (LEB)
- Synchronized Slope Compensation
- Internal Open-Loop Protection
- Gate Output Maximum Voltage Clamp: 18V
- V_{DD} Under-Voltage Lockout (UVLO)
- V_{DD} Over-Voltage Protection (OVP)
- Programmable Over-Temperature Protection (OTP)
- Internal Latch Circuit (OTP)
- Built-In 5ms Soft-Start Function
- Constant Power Limit (Full AC Input Range)
- Internal OTP Sensor with Hysteresis

Applications

General-purpose, switch-mode power supplies and flyback power converters, including:

- Power Adapters
- Open-Frame Switch-Mode Power Supply (SMPS)

Introduction

The highly integrated FAN6753 series of PWM controllers provides several features to enhance the performance of flyback converters.

To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency at light-load conditions. To avoid acoustic-noise problems, the minimum PWM frequency is set above 22KHz. This green-mode function enables the power supply to meet international power conservation requirements. With the internal high-voltage startup circuitry, the power loss due to bleeding resistors is also eliminated. To further reduce power consumption, FAN6753 is manufactured using the BiCMOS process, which allows an operating current of only 2.7mA.

Built-in synchronized slope compensation achieves stable peak-current-mode control. The proprietary external line compensation ensures a constant output-power limit over a wide AC input voltage range, from $90V_{AC}$ to $264V_{AC}$.

FAN6753 provides many protection functions. In addition to cycle-by-cycle current limiting, the internal open-loop protection circuit ensures safety should an open-loop or output short-circuit failure occur.

	OVP (V_{DD})	OLP (FB)	External Latch (LATCH)
FAN6753	Auto Restart	Auto Restart	Latch

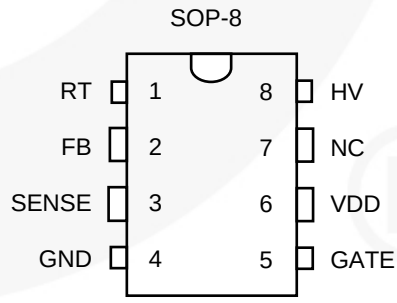

Figure 1. Pin Configuration (Top View)

Typical Application

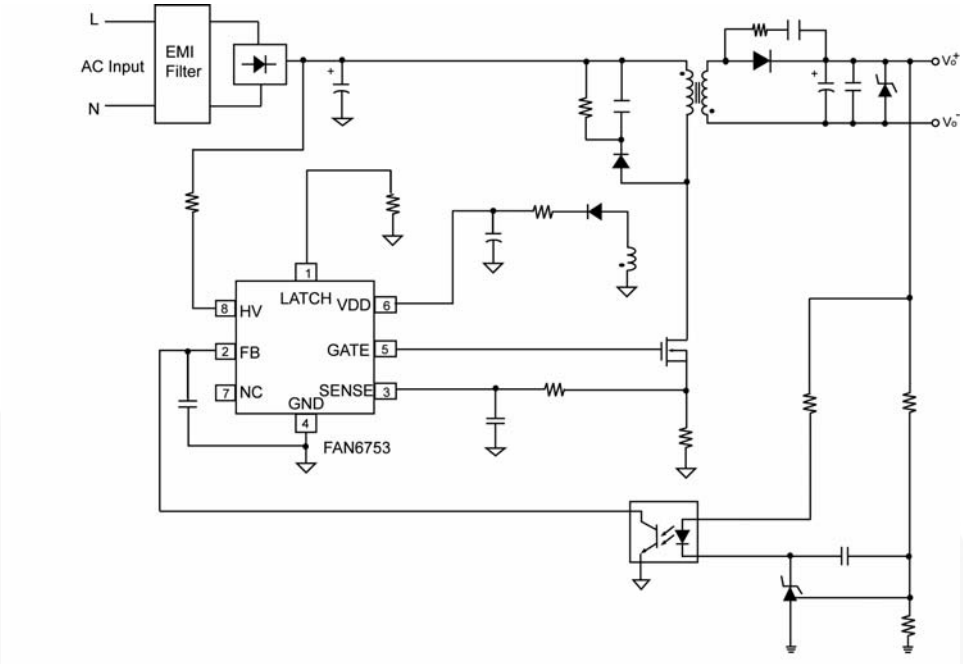

Figure 2. Typical Application

Block Diagram

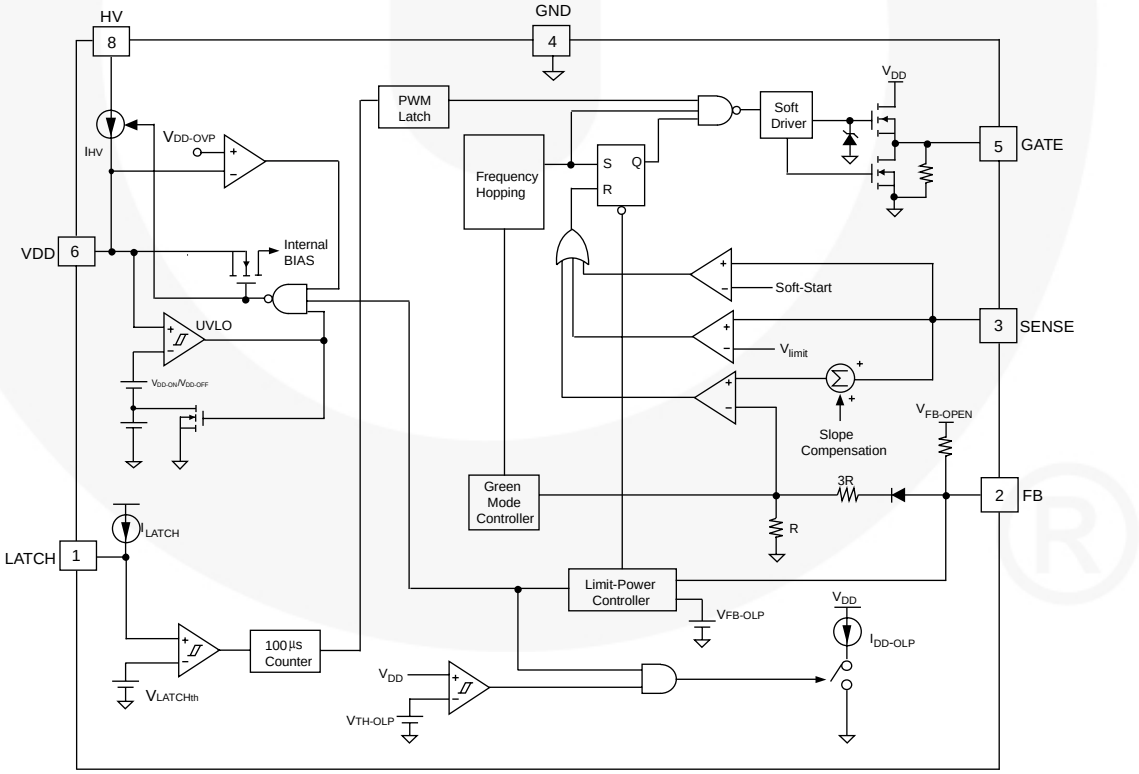

Figure 3. Functional Block Diagram

Internal Block Operation

Startup Circuitry

When the power is turned on, the internal current source (typically 2mA) charges the hold-up capacitor C_1 through a startup resistor R_{HV}. During the startup sequence, the V_{AC} provides a startup current of about 2mA and charges the V_{DD} capacitor C_1. R_{HV} and D2 are series connections and can be directly connected by V_{AC} to the HV pin. As the VDD pin reaches the start threshold voltage V_{DD-ON}, the FAN6753 activates and signals the MOSFET. The high-voltage source current is switched off and the supply current is drawn from the auxiliary winding of the main transformer, as shown in Figure 4. For higher 6KV surge test, R_{HV} of 100KΩ or above is recommended.

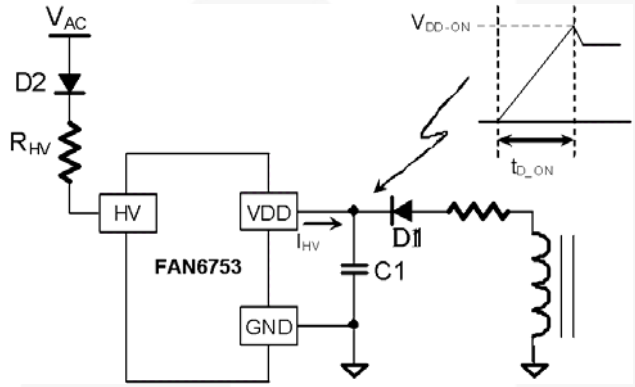

Figure 4. Startup Circuit for Power Transfer

When the supply current is drawn from the transformer, it draws a leakage current of about 1μA from the HV pin. The maximum power dissipation of the R_{HV} is:

$$P_{R_{HV}} = I_{HV-LC(Typ.)}^{2} \times R_{HV} \quad (1)$$

where I_{HV-LC} is the supply current drawn from HV pin.

$$P_{R_{HV}} = 1\mu A^2 \times 100K\Omega \cong 0.1\mu W \quad (2)$$

Soft Start

For many applications, it is necessary to minimize the inrush current during the startup period. The built-in 5ms soft-start circuit significantly reduces the startup current spike and output-voltage overshoot.

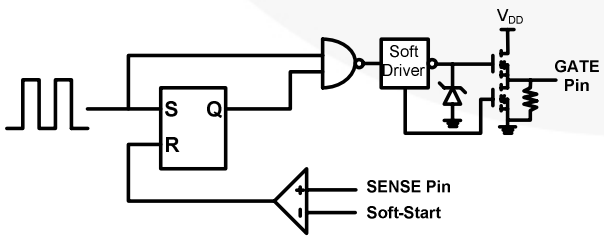

Figure 5. Soft-Start Circuit

Under-Voltage Lockout (UVLO)

The FAN6753 has a voltage detector on the VDD pin to ensure that the chip has enough power to drive the MOSFET. Figure 6 shows a hysteresis of the turn-on and turn-off threshold levels and an open-loop-release voltage.

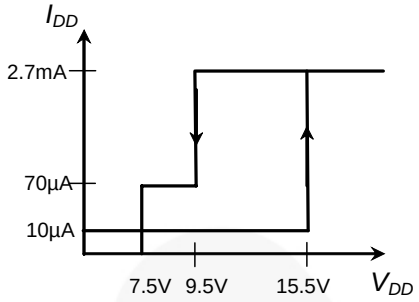

Figure 6. UVLO Specification

The turn-on and turn-off thresholds are internally fixed at 15.5V and 9.5V. During startup, the V_{DD} capacitor must be charged to 15.5V to enable the IC. The capacitor continues to supply the V_{DD} until the energy can be delivered from the auxiliary winding of the main transformer. The V_{DD} must not drop below 9.5V during startup.

If the secondary output short circuit or the feedback loop is open, the FB pin voltage rises rapidly toward the open-loop voltage, $V_{FB-OPEN}$. If the FB voltage remains above V_{FB-OLP} and lasts for t_{D-OLP}, the FAN6753 stops emitting output pulses and enters auto-restart mode. To further limit the input power under a short-circuit or open-loop condition, a special two-step UVLO mechanism prolongs the discharge time of the V_{DD} capacitor. Figure 7 shows the traditional UVLO method, along with the special two-step UVLO method. In the two-step UVLO mechanism, an internal sinking current, I_{DD-OLP}, pulls the V_{DD} voltage toward the V_{DD-OLP}. This sinking current is disabled after the V_{DD} drops below V_{DD-OLP}; after which the V_{DD} voltage is again charged towards V_{DD-ON}. With the two-step UVLO mechanism, the average input power during a short-circuit or open-loop condition is greatly reduced. As a result, over-heating does not occur.

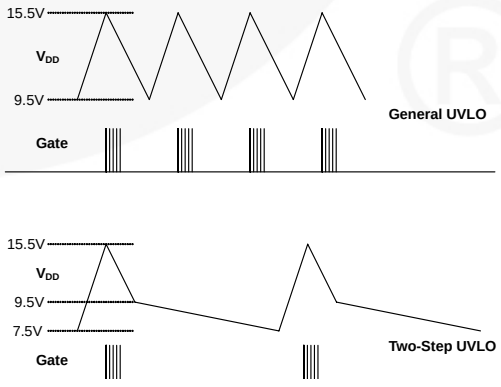

Figure 7. UVLO Effect

FB Input

The FAN6753 is designed for peak-current-mode control. A current-to-voltage conversion is accomplished externally with current-sense resistor R_S. Under normal operation, the FB level controls the peak inductor current:

$$I_{PEAK} = \frac{V_{FB} - 0.6}{4 \times R_S} \quad (3)$$

where V_{FB} is the voltage on the FB pin and 4 is an internal divider ratio.

When V_{FB} is less than 0.6V, the FAN6753 terminates the output pulses.

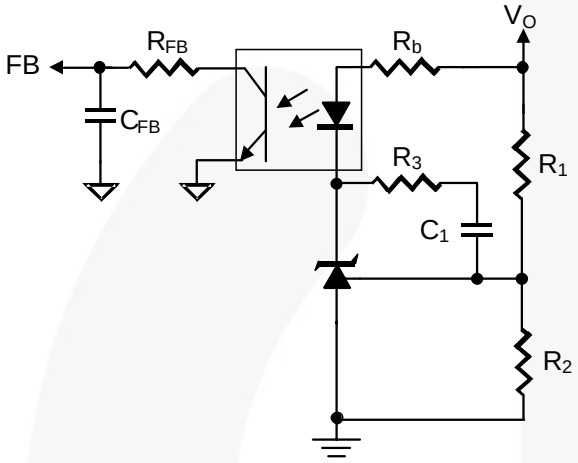

Figure 8. Feedback Circuit

Figure 8 is a typical feedback circuit consisting mainly of a shunt regulator and an opto-coupler. R_1 and R_2 form a voltage divider for the output-voltage regulation. R_3 and C_1 are adjusted for control-loop compensation. A small-value RC filter (e.g. R_{FB}= 47Ω, C_{FB}= 1nF) placed on the FB pin to the GND can further increase stability. The maximum sourcing current of the FB pin is 1.5mA. The phototransistor must be capable of sinking this current to pull the FB level down at no load. The value of the biasing resistor, R_b, is determined as follows:

$$\frac{V_{OUT} - V_D - V_Z}{R_b} \cdot K \geq 1.5mA \quad (4)$$

where:

V_D is the drop voltage of photodiode, approximately 1.2V;

V_Z is the minimum operating voltage, 2.5V of the shunt regulator; and

K is the current transfer rate (CTR) of the opto-coupler.

For an output voltage V_{OUT} = 5V, with CTR = 100%, the maximum value of R_b is 860Ω.

Built-In Slope Compensation

A flyback converter can be operated in Discontinuous Current Mode (DCM) or Continuous Current Mode (CCM). There are many advantages when operating the converter in CCM. With the same output power, a converter in CCM exhibits a smaller peak inductor current than one in DCM. Therefore, a small-sized transformer and a low-rated MOSFET can be applied. On the secondary side of the transformer, the RMS output current of DCM can be twice that of CCM. Larger wire gauge and output capacitors with larger ripple-current ratings are required. DCM operation also results in a higher output voltage spike. A large LC filter is added. Therefore, a flyback converter in CCM achieves better performance with lower component cost.

Despite the above advantages of CCM operation, there is one concern—stability. In CCM operation, the output power is proportional to the average inductor current, while the peak current remains controlled. This causes sub-harmonic oscillation when the PWM duty cycle exceeds 50%. Adding slope compensation (reducing the current-loop gain) is an effective way to prevent oscillation. The FAN6753 introduces a synchronized positive-going ramp (V_{SLOPE}) in every switching cycle to stabilize the current loop. Therefore, FAN6753 helps design a cost-effective, highly efficient, compact, flyback power supply that operates in CCM without additional external components.

The positive ramp added is:

$$V_{SLOPE} = V_{SL} \bullet D \quad (5)$$

where V_{SL} = 0.33V and D = duty cycle.

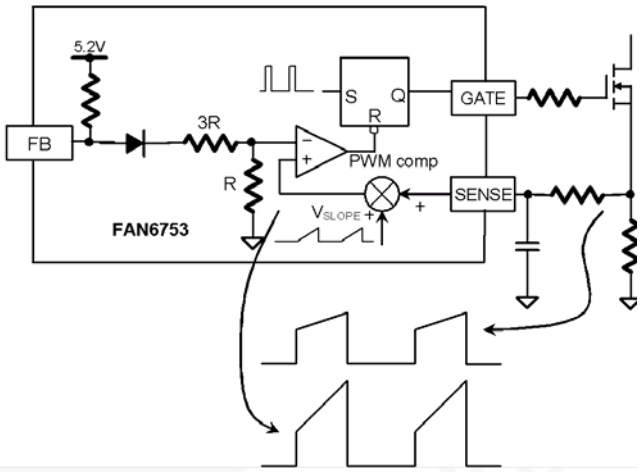

Figure 9. Synchronized Slope Compensation

Constant Output-Power Limit

The maximum output power of a flyback converter can generally be determined from the current-sense resistor R_S. When the load increases, the peak inductor current increases accordingly. When the output current arrives at the protection value, the Output-Current-Protection (OCP) comparator dominates the current-control loop. OCP occurs when the current-sense voltage reaches the threshold value. The output GATE driver is turned off after a small propagation delay, t_{PD}. The delay time results in unequal power-limit levels under universal input. A sawtooth power limiter (saw limiter) is designed to solve the unequal power limit problem. As shown in Figure 10, the saw limiter is designed as a positive ramp signal (V_{limit_ramp}) and is fed into the inverting input of the OCP comparator. This results in a lower current limit at high-line inputs than at low-line inputs. However, with the fixed propagation delay t_{PD}, the peak primary current would be the same for various line-input voltages. Therefore, the maximum output power can remain a constant value within a wide input voltage range without adding any external circuitry.

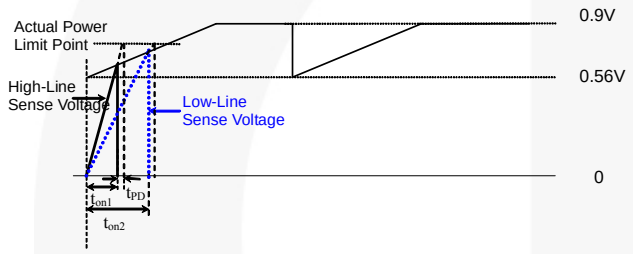

Figure 10. Constant Power-Limit Compensation

Leading-Edge Blanking (LEB)

A voltage signal proportional to the MOSFET current develops on the current-sense resistor R_S. Each time the MOSFET is turned on, a spike induced by the diode reverse recovery and the output capacitances of the MOSFET and diode appears on the sensed signal. A leading-edge blanking time of about 140ns is introduced to avoid premature termination of the MOSFET by the spike. Therefore, only a small-value RC filter (e.g. 100Ω + 470pF) is required between the SENSE pin and R_S. Still, a non-inductive resistor for the R_S is recommended.

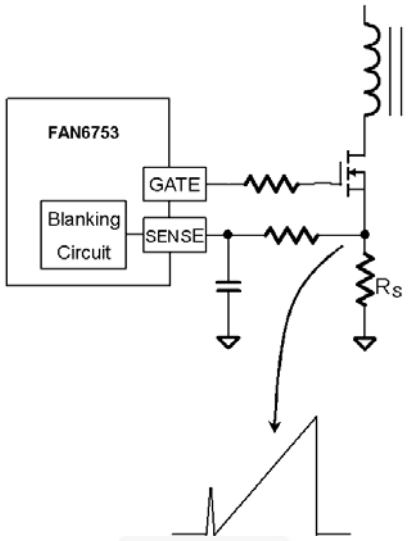

Figure 11. LEB Circuit

Open-Loop Protection (OLP)

The FAN6753 contains an open-loop protection function. If the output load is higher than the maximum output current, the output voltage drops and the feedback error amplifier is saturated. Once the FB voltage trips the OLP threshold of 4.8V for longer than 56ms, the protection is activated to turns off the gate output to stop the switching of power circuit. As shown in Figure 1, the FB voltage is compared with 4.8V reference voltage. If the FB voltage is higher than 4.8V, the OLP timer starts counting. If the OLP condition persists for 56ms, the OLP signal could be asserted. This protection is reset after UVLO.

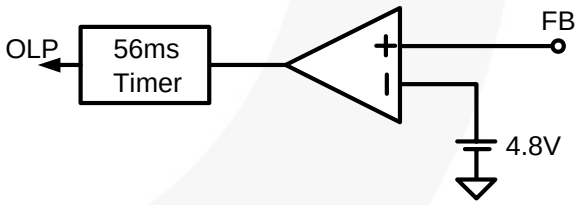

Figure 12. Open-Loop Protection Circuit

Output Driver / Soft Driving

The output stage is a fast totem-pole gate driver capable of directly driving an external MOSFET. An internal Zener diode clamps the driver voltage under 18V to protect the MOSFET against over-voltage. By integrating special circuits to control the slew rate of switch-on rising time, the external resistor R_G may not be necessary to reduce switching noise, improving Electromagnetic Interference (EMI) performance.

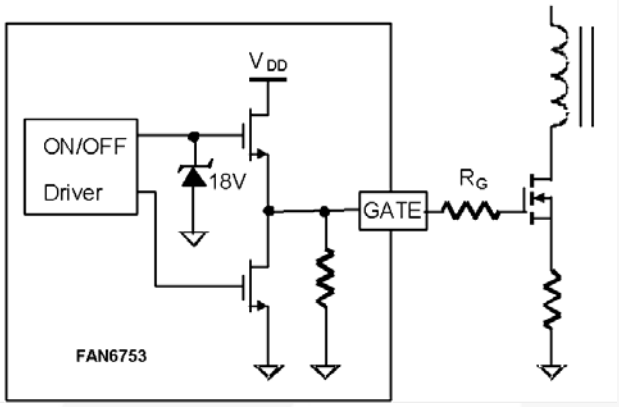

Figure 13. Gate Driver

External Latch Function (LATCH Pin)

The LATCH pin can be used to control the FAN6753 entering latch mode by pulling this pin over 5.2V for 100μs. If floating, the LATCH pin is internally pulled HIGH to 3.5V. It is not recommended to float or short the LATCH pin to GND. This pin also includes a test mode to disable the jitter function. LATCH pin internally sources 100μA, so place a resistor in series to GND. Do not let this voltage exceed 5.2V for the FAN6753 to function normally.

Over-Temperature Protection (OTP)

The built-in temperature-sensing circuit shuts down PWM output once the junction temperature exceeds 135°C. While PWM output is shut down, V_{DD} gradually drops to the UVLO voltage (around 7.5V). V_{DD} then charges up to the startup threshold voltage of 15.5V through the startup resistor until PWM output is restarted. This hiccup-mode protection occurs repeatedly as long as the temperature remains above 130°C. The temperature hysteresis window for the OTP circuit is 25°C.

Printed Circuit Board Layout

Current, voltage, and switching frequency make PCB layout and design very important. Good PCB layout minimizes excessive EMI and prevents the power supply from being disrupted during surge/ESD tests. The following are some general guidelines:

- For better EMI performance and to reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C_{bulk} first, then to switching circuits.
- The high-frequency current loop is found in the loop C_{bulk} – Transformer – MOSFET – R_S – C_{bulk} in Figure 14. The area enclosed by this current loop should be as small as possible. Keep the traces (especially 4→1) short, direct, and wide. High-voltage drain traces related to the MOSFET and RCD snubber should be kept far from control circuits to prevent unnecessary interference. If a heatsink is used for the MOSFET, grounding the heatsink is recommended.
- As indicated by 3 in Figure 14, the control circuits' ground should be connected first, then to other circuitry.
- As indicated by 2 in Figure 14, the area enclosed by the transformer auxiliary winding, D_1, and C_1 should also be kept small. Place C_1 close to FAN6753 for good decoupling.

Two suggestions with pros and cons for ground connections are recommended.

- GND3→2→4→1: Possible method for circumventing the sense signals and common impedance interference.
- GND3→2→1→4: Potentially better for ESD testing where a ground is not available for the power supply. The charges for the ESD discharge path go from secondary, through the transformer stray capacitance, to the GND2 first. Then, the charges go from GND2 to GND1 and back to the mains. It should be noted that control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high-frequency impedance and help increase ESD immunity.
- Should a Y-cap between primary and secondary be required, the Y-cap should be connected to the positive terminal of the C_{bulk} (V_{DC}). If this Y-cap is connected to the primary GND, it should be connected to the negative terminal of the C_{bulk} (GND1) directly. Point discharge of the Y-cap also helps with ESD. However, according to safety requirements, the creepage between the two pointed ends should be at least 5mm.

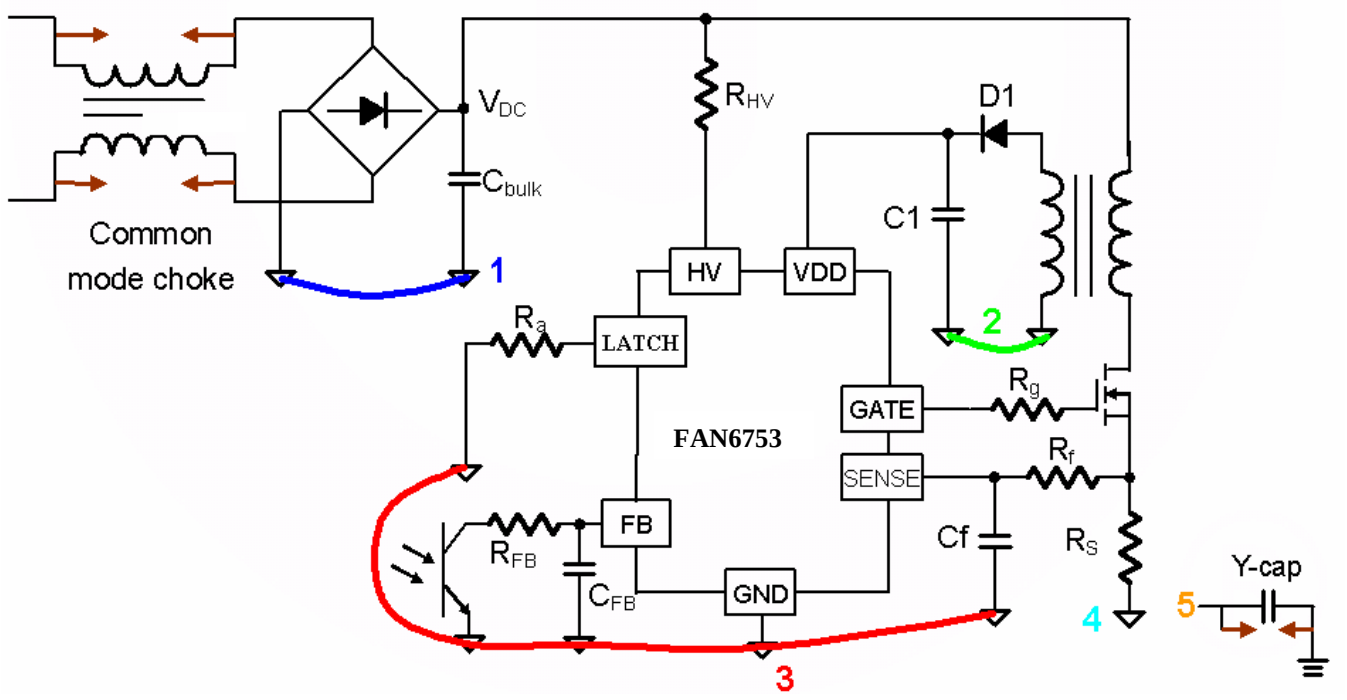

Figure 14. Layout Considerations

PCB Layout Suggestions for LCD monitor / TV Application:

1. Safety distance for EMI loop requirement in LCD monitor /TV application:
   UL60950 safety distance for lightening surge standard.

Table G.2 -- Minimum clearance up to 2 000 m above sea level

Required WITHSTAND VOLTAGE V peak or d.c.	CLEARANCES in millimetres				
	Minimum CLEARANCES in air				
	FUNCTIONAL INSULATION	BASIC and SUPPLEMENTARY INSULATION		REINFORCED INSULATION	
Up to 400	0,1	0,2	(0,1)	0,4	(0,2)
800	0,1	0,2		0,4	
1 000	0,2	0,3		0,6	
1 200	0,3	0,4		0,8	
1 500	0,5			1,6	(1)
2 000	1	1,3	(1)	2,6	(2)
2 500	1,5	2	(1,5)	4	(3)
3 000	2	2,6	(2)	5,2	(4)
4 000	3	4	(3)	6	
6 000	5,5	7,5		11	
8 000	8	11		16	
10 000	11	15		22	
12 000	14	19		28	
15 000	18	24		36	
25 000	33	44		66	
40 000	60	80		120	
50 000	75	100		150	
60 000	90	120		180	
80 000	130	173		260	
100 000	170	227		340	

1) Except in PRIMARY CIRCUITS in G.4 a), linear interpolation is permitted between the nearest two points, the calculated minimum CLEARANCES being rounded up to the next higher 0,1 mm increment.
2) The values in parentheses are applicable only if manufacturing is subjected to a quality control programme, that provides at least the same level of assurance as the example given in clause R.2. In particular, DOUBLE and REINFORCED INSULATION shall be subjected to ROUTINE TESTS for electric strength.
3) Compliance with a CLEARANCE value of 8,4 mm or greater for SECONDARY CIRCUITS is not required if the CLEARANCE path is:
– entirely through air; or
– wholly or partly along the surface of an insulation of Material Group I;
and the insulation involved passes an electric strength test according to 5.2.2, using:
• an a.c. test voltage whose r.m.s. value is equal to 1,06 times the PEAK WORKING VOLTAGE; or
• a d.c. test voltage equal to the peak value of the a.c. test voltage prescribed above.
If the CLEARANCE path is partly along the surface of a material that is not of Material Group I, the electric strength test is conducted in the air gap only.

The UL60950 standard defines the safety distance for product operation where voltage is under 600V. The following table details distance for the power system PCB layout requirements from LCD monitor / TV specifications.

Application Surge Voltage (V)	Location	Layout Distance	Design Rule (Practical)
30000	L-FG / N-FG / L-N	2mm	2.6mm
4000V	L-FG / N-FG / L-N	3mm	4mm
5000V	L-FG / N-FG / L-N	4mm	5mm
6000V	L-FG / N-FG / L-N	5.5mm	6mm
9000V	L-FG / N-FG / L-N	9mm	9mm
12000V	L-FG / N-FG / L-N	14mm	14mm

From the surge discharge loop function, it is necessary to lead the surge energy to ground. Two concepts can solve the issue:

- Provide enough distance (follow no.1).
- Use air and gap to replace SPA tube and reduce the cost by PCB layout.
- The location is as the table below describes:

Location	Safety Distance(CL)	Gap Width	Discharge (Gap / Air)(Point Discharge)
L -> FG(SG)	Table G.2	1mm	Yes
N -> FG(SG)	Table G.2	1mm	Yes
YC1 -> FG	Table G.2	1mm	Yes
YC2 -> FG	Table G.2	1mm	Yes
CM CHOKE	Table G.2	1mm	Yes

The ground path has the shortest loop and largest area in the primary side. (The PCB layout trace is the good loop.)

Use the AC inlet's mechanic component (ground clip and heat sink) to reduce the ground impedance and lead the surge energy to ground path in the building.

Design Example, 19V/3.42A for NB Adaptor

Following is the specification of the design example:
V_{IN} min = 100 V_{DC} (bulk valley in low-line conditions)
V_{IN} max = 375 V_{DC}
V_{OUT} = 19V
I_{OUT} = 3.42A
Operating mode is CCM
η= 0.8
f_{SW} = 65 kHz

Follow below steps to design a transformer:

1. Turn Ratio.
The MOSFET BV_{dss} dictates the amount of reflected voltage needed. Considering a 600V MOSFET and a 15% de-rating factor, limit the maximum drain voltage to:

$$V_{DS\_max} = 600 \bullet 0.85 = 510V \quad (6)$$

Knowing a maximum bulk voltage of 375V, the clamp voltage must be set to:

$$V_{clamp} = 510 - 375 = 135V \quad (7)$$

Based on the above level, adopt a headroom between the reflected voltage and the RCD clamp level of 50V. If this headroom is too small, a high dissipation can occur on the RCD clamp network and efficiency suffers. A leakage inductance of around 1% of the magnetizing value should give good results with this choice (kc = 1.6). The turn ratio between primary and secondary is:

$$(V_{OUT} + V_f)/n = V_{clamp}/kc \quad (8)$$

Solving for n gives:

$$n = N_S/N_P = kc \bullet (V_{OUT} + V_f)/V_{clamp} = 1.6 \bullet (19 + 0.8)./135 = 0.234 \quad (9)$$

Round it to 0.25 or 1/n = 4.

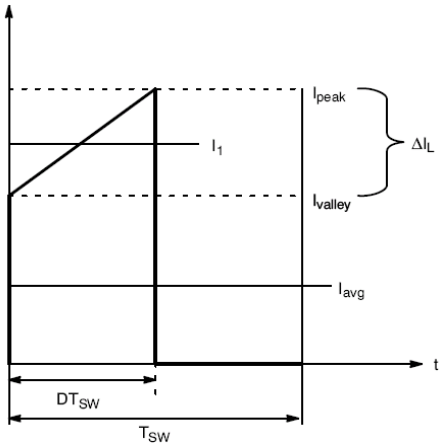

Figure 15. Primary Inductance Current Evolution in CCM

2. Calculate the maximum operating duty-cycle for this flyback converter operated in CCM:

$$d\max = (V_{OUT}/n)/(V_{OUT}/n + V_{IN\_max}) = (19 \bullet 4)/(19 \bullet 4 + 100) = 0.43 \quad (10)$$

In this equation, the CCM duty-cycle does not exceed 50%. The design should therefore be free of sub-harmonic oscillations in steady-state conditions.

3. To obtain the primary inductance, use the following equation, which expresses the inductance in relationship to a ripple factor K_{RF}. This coefficient dictates the depth of the CCM operation.

$$L = (V_{IN\_min} \bullet d\max)^2/(f_{SW} \bullet K_{RF} \bullet Pin) \quad (11)$$

where $K_{RF} = \triangle I_L/I_1$ and defines the amount of ripple desired in CCM (*see Figure 15*).

- Small K_{RF}: deep CCM, implying a large primary inductance, a low bandwidth, and a large leakage inductance.
- Large K_{RF}: approaching BCM, where the RMS losses are the worse, but smaller inductance, leading to a better leakage inductance.

Selecting a K_{RF} factor of 0.8 (40% ripple) ensures good operation over universal mains. It leads to an inductance of:

$$L = (100 \bullet 0.43)^2/(65k \bullet 0.8 \bullet 82) = 433\mu H \quad (12)$$

$$\Delta I_L = (V_{IN\_min} \bullet d_{max})/(f_{SW} \bullet L) = (100 \bullet 0.43)/(65k \bullet 433\mu H) = 1.53A\ peak\text{-}to\text{-}peak \quad (13)$$

The peak current can be evaluated as:

$$I_{IN\_avg} = P_{OUT}/(\eta \bullet V_{IN\_min}) = (19 \bullet 3.42)/(0.8 \bullet 100) = 812mA \quad (14)$$

$$I_{PEAK} = I_{IN\_avg}/d_{max} + \Delta I_L/2 = 0.813/0.43 + 1.53/2 = 2.66A \quad (15)$$

Based on Figure 15, I_1 can also be calculated as:

$$I_1 = I_{peak} - \Delta I_L/2 = 2.66 - (1.53/2) = 1.9A \quad (16)$$

The valley current is found to be:

$$I_{valley} = I_{peak} - \Delta I_L = 2.66 - 1.53 = 1.13A \quad (17)$$

4. Based on the above, evaluate the RMS current circulating in the MOSFET and the sense resistor:

$$I_{d\_rms} = I_1 \bullet \sqrt{d} \bullet \sqrt{(1 + 1/3 \bullet (\Delta I_L)/(2 \bullet I_1))^2} = 1.9 \times 0.66 \bullet \sqrt{(1 + 1/3 \bullet (1.53/(2 \bullet 1.9))^2)} = 1.29A \quad (18)$$

5. The current peaks to 2.66A. If the desired OCP is 120% of I_{peak} and FAN6753's V_{limit_L} clamps 0.9V drop across the sense resistor, compute its value as:

$$R_{sense} = 0.9V/(2.66A \bullet 120\%) = 0.282\Omega \quad (19)$$

Using Equation 18, the power dissipated in the sense element reaches:

$$P_{sense} = R_{sense} \bullet I_{d\_rms}^2 = 0.282 \bullet 1.29^2 = 470mW \quad (20)$$

Related Datasheets

FAN6753 — Highly Integrated Green-Mode PWM Controller

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