

ActivePSR™ Primary Switching Regulators

FEATURES

- Multiple Patent-Pending Primary Side Regulation Technology
- No Opto-coupler
- Best-in-Class Constant Voltage, Constant Current Over All Accuracy
- Minimum External Components
- Integrated Line and Primary Inductance Compensation
- Integrated Output Cord Resistance Compensation
- Line Under-Voltage Protection
- Flyback Topology in DCM Operation
- Complies with all Global Energy Efficient Regulations: 0.3W Standby Power and CEC Average Efficiency
- SIP-4 and SOT23-5 Packages

APPLICATIONS

- Chargers for Cell Phones, PDAs, MP3, Portable Media Players, DSCs, and Other Portable Devices and Appliances
- RCC Adapter Replacements
- Linear Adapter Replacements
- Standby and Auxiliary Supplies

GENERAL DESCRIPTION

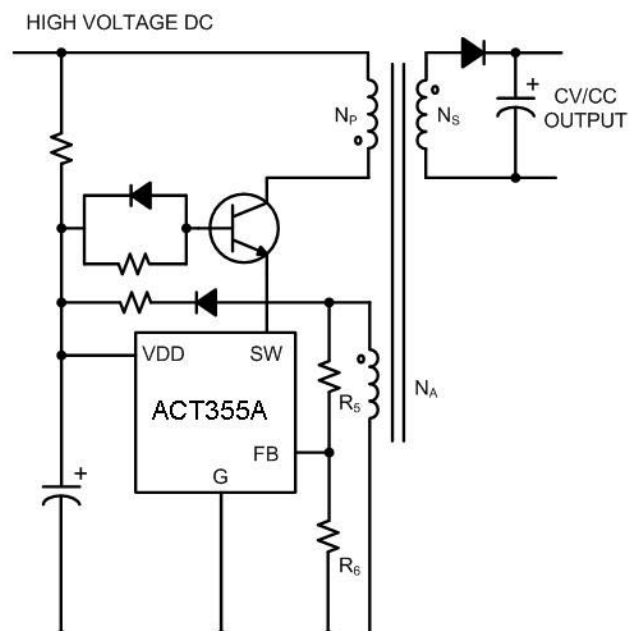
The ACT355A belongs to the high performance, multiple patent-pending *ActivePSR™* Family of universal-input AC/DC off-line controllers for battery charger and adapter applications. It is designed for the Flyback topology working in a discontinuous conduction mode (DCM). In addition to being the industry's most accurate primary side regulator, the ACT355A meets all of the global energy efficiency regulations (CEC, European Blue Angel, and US Energy Star standards) while using very few external components.

The ACT355A ensures safe operation with complete protection against all fault conditions. Built-in protection circuitry is provided for output short-circuit, line under-voltage, and over-temperature conditions.

The ACT355A *ActivePSR™* is optimized for cost-sensitive applications, and utilizes Active-semi's proprietary primary-side feedback architecture to provide accurate constant voltage, constant current (CV/CC) regulation without the need of an opto-coupler or reference device. Integrated line and primary inductance compensation circuitry provides accurate constant current operation despite wide variations in line voltage and primary inductance. Integrated output cord resistance compensation further enhances output accuracy. These products achieve excellent regulation and transient response, yet requires less than 300mW of standby power.

The ACT355A is optimized for 2.5W to 3.5W applications (such as 5V/500mA to 5V/700mA CV/CC chargers). It is available in space-saving 4-pin SIP-4 and 5-pin SOT23-5 packages.

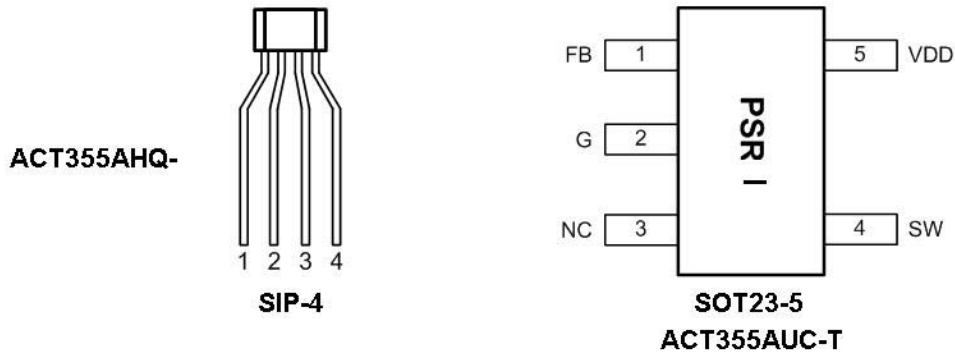
Figure 1:
Typical Application Circuit



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING METHOD	TOP MARK
ACT355AHQ-A	-40°C to 85°C	SIP-4	4	AMMO	ACT355AHQ
ACT355AUC-T	-40°C to 85°C	SOT23-5	5	TAPE & REEL	PSRC

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER		PIN NAME	PIN DESCRIPTION
ACT355AHQ-A	ACT355AUC-T		
1	1	FB	Feedback Pin. Connect to a resistor divider network from the auxiliary winding.
2	5	VDD	Power supply.
3	4	SW	Switch Driver. Connect this pin to the emitter of the power NPN transistor or source of the power MOSFET.
4	2	G	Ground.
	3	NC	No Connection.

ABSOLUTE MAXIMUM RATINGS[Ⓞ]

PARAMETER		VALUE	UNIT
VDD to G		-0.3 to +22	V
Maximum Continuous VDD Current		20	mA
FB to G		-0.3 to +6	V
SW to G		-0.3 to +22	V
Continuous SW Current		Internally limited	A
Junction to Ambient Thermal Resistance (θ_{JA})	SIP-4	200	°C/W
	SOT23-5	190	
Maximum Power Dissipation	SIP-4 (derate 5mW/°C above $T_A = 50^\circ\text{C}$)	0.5	W
	SOT23-5 (derate 5.3mW/°C above $T_A = 50^\circ\text{C}$)	0.53	
Operating Junction Temperature		-40 to 150	°C
Storage Temperature		-55 to 150	°C
Lead Temperature (Soldering, 10 sec)		300	°C

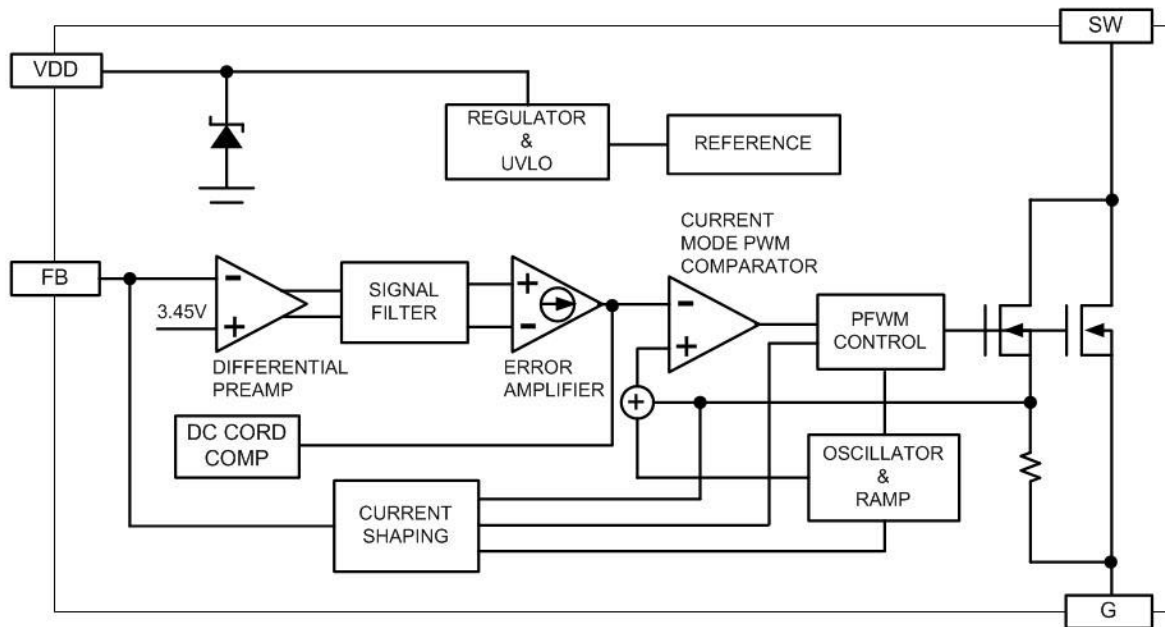
Ⓞ: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{DD} = 15\text{V}$, $V_{OUT} = 5\text{V}$, $L_P = 1.7\text{mH}$, $N_P = 130$, $N_S = 10$, $N_A = 32$, $T_A = 25^\circ\text{C}$, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD Turn-On Voltage	V_{DDON}	V_{DD} Rising		20.7		V
VDD Turn-Off Voltage	V_{DDOFF}	V_{DD} Falling	7	7.5	8	V
VDD Clamp Voltage	$V_{DDCLAMP}$	10mA		21.7		V
Supply Current	I_{DD}			1	2	mA
Start Up Supply Current	I_{DDST}	$V_{DD} = 15\text{V}$, before turn-on		30	55	μA
Switching Frequency	f_{SW}	Circuit of Figure 3, 100% V_{OUTCV}		40		kHz
		Circuit of Figure 3, 50% V_{OUTCV}		20		
Effective FB Feedback Voltage	V_{FB}	FB in Regulation	3.38	3.45	3.52	V
Dynamic Load Step Response	ΔV_{OUT}	$\Delta I_{OUT} = 0$ to 75% Full Load			10	%-2ms
Output Cord Resistance Compensation		Maximum Output Power		+3.1		%
Primary Current Limit	I_{LIM}			340		mA
Maximum Duty Cycle	D_{MAX}	$I_{SW} = 10\text{mA}$	70	75	82	%
Switch On-Resistance	R_{ON}	$I_{SW} = 50\text{mA}$		3.5	5	Ω
SW Rise Time		1nF load, 15 Ω pull-up		30		ns
SW Fall Time		1nF load, 15 Ω pull-up		20		ns
SW Off Leakage Current		Switch in off-state, $V_{SW} = 22\text{V}$		1	10	μA
Over-Temperature Threshold				160		°C

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

As shown in the *Functional Block Diagram*, the ACT355A feedback regulation is done via several circuit blocks to pre-amplify the FB pin error voltage relative to an internal reference, filter out the switching transients, and integrate the resulting useful differential error voltage for current mode PFWM (Pulse Frequency and Width Modulation) control.

SW is a driver output that drives the emitter of an external high voltage NPN transistor or N-channel MOSFET. This emitter-drive method takes advantage of the high V_{CBO} of the transistor, allowing a low cost transistor such as '13003 ($V_{CBO} = 700V$) or '13002 ($V_{CBO} = 600V$) to be used for a wide AC input range.

Startup Mode

VDD is the power supply terminal for the IC. During startup, the IC typically draws 30 μ A supply current. The bleed resistor from the rectified high voltage DC rail supplies current to VDD until it exceeds the V_{DDON} threshold of 20.7V. At this point, the IC enters normal operation when switching begins and the output voltage begins to rise. The VDD bypass capacitor must supply the IC and the NPN base drive until the output voltage builds up enough to provide power from the auxiliary winding to sustain the VDD. The V_{DDOFF} threshold is 7.5V, and therefore, the voltage on the VDD capacitor must

not drop more than 11V while the output is charging up.

Constant Voltage (CV) Mode

In constant voltage operation, the IC captures the auxiliary flyback signal at FB pin through a resistor divider network R_5 and R_6 in Figure 1. The FB pin is pre-amplified against the reference voltage, and the secondary side output voltage error is extracted based on Active-Semi's proprietary filter architecture. This error signal is then integrated by the Error Amplifier.

When the secondary output voltage is above regulation, the Error Amplifier output voltage decreases to reduce the switch current. When the secondary side is below regulation, the Error Amplifier output voltage increases to ramp up the

$$V_{OUTCV} = 3.45V \times \left(1 + \frac{R_5}{R_6}\right) \left(\frac{N_S}{N_A}\right) - V_F \quad (1)$$

switch current to bring the secondary output back to regulation. The output regulation voltage is determined by the following relationship:

where R_5 and R_6 are top and bottom feedback resistor, N_S and N_A are numbers of transformer secondary and auxiliary turns, and V_F is the rectifier diode forward drop voltage at approximately 0.1A bias. The ACT355A includes internal feedback loop compensation to simplify application circuit design.

Constant Current (CC) Mode

When the secondary output current reaches a level set by the internal current limiting circuit, the IC enters current limit condition and causes the secondary output voltage to drop. As the output voltage decreases, so does the flyback voltage in a proportional manner. Internal current shaping circuitry adjusts the switching frequency based on the flyback voltage so that the transferred power remains proportional to the output voltage, resulting in a constant secondary side output current profile.

$$I_{OUTCC} = \frac{1}{2} L_P \times I_{LIM}^2 \left(\frac{\eta \times f_{SW}}{V_{OUTCV}} \right) \quad (2)$$

The energy transferred to the output during each switching cycle is $\frac{1}{2}(L_P \times I_{LIM}^2) \times \eta$, where L_P is the transformer primary inductance, I_{LIM} is the primary peak current, and η is the conversion efficiency. From this formula, the constant output current can be derived:

where f_{SW} is the nominal switching frequency and V_{OUTCV} is the nominal secondary output voltage. The constant current operation typically extends down to lower than 40% of output voltage regulation.

Light Load Mode

When the secondary side output load current decreases to an internally set light load level, the IC's switching frequency is also reduced to save power. This enables the application to meet all current green energy standards. The actual minimum switching frequency is programmable with a small dummy load (while still meeting standby power).

Short Circuit Mode

When the secondary side output is short circuited, the ACT355A enters hiccup mode operation. In this condition, the auxiliary supply voltage collapses and the VDD voltage drops below the V_{DDOFF} threshold. This turns off the IC and causes it to restart. This hiccup behavior continues until the short circuit is removed.

Loop Compensation

The ACT355A integrates patent-pending loop compensation circuitry for simplified application design, optimized transient response, and minimal external components.

Primary Inductance Compensation

The ACT355A includes patent-pending built-in primary inductance compensation to maintain constant current regulation despite variations in transformer manufacturing.

Peak Inductor Current Limit Compensation

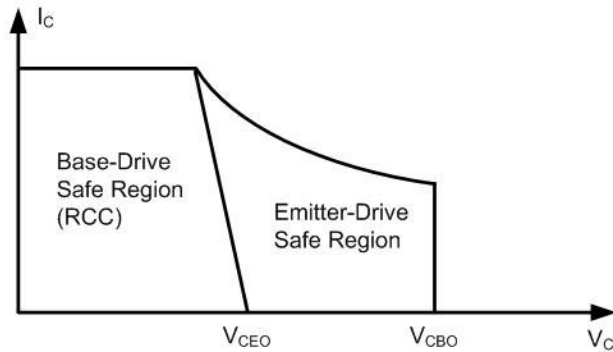
The ACT355A includes patent-pending peak inductor current limit compensation to achieve constant input power over wide line and wide load range.

Output Cord Resistance Compensation

The ACT355A provides automatic output cord resistance compensation during constant voltage regulation, monotonically adding an output voltage correction up to a typical correction of 3.1% at full power. This feature allows for better output voltage accuracy by compensating for the output voltage droop due to the output cord resistance.

APPLICATIONS INFORMATION

Figure 2:
NPN Transistor Reverse Bias Safe Operation Area



External Power Transistor

The ACT355A allows a low-cost high voltage power NPN transistor such as '13003 or '13002 to be used safely in flyback configuration. The required collector voltage rating for $V_{AC} = 265V$ with full output load is at least 600V to 700V. As seen from Figure 2, NPN Reverse Bias Safe Operation Area,

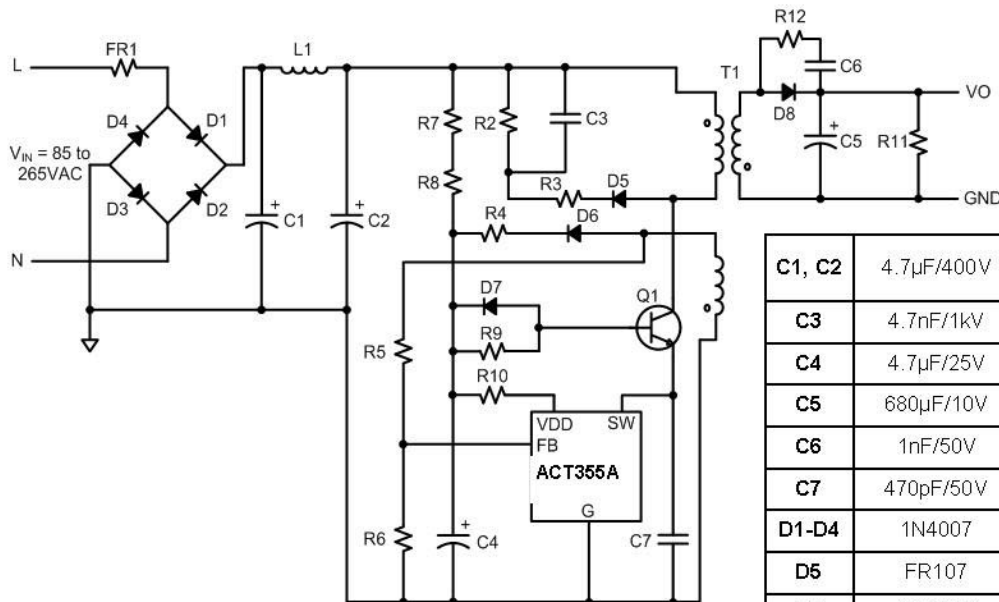
the breakdown voltage of an NPN is significantly improved when it is driven at its emitter. Thus, the ACT355A+'13002 or '13003 combination meets the necessary breakdown safety requirement. Table 1 lists the breakdown voltage of some transistors appropriate for use with the ACT355A.

The power dissipated in the NPN transistor is equal to the collector current times the collector-emitter voltage. As a result, the transistor must always be in saturation when turned on to prevent excessive power dissipation. Select an NPN transistor with sufficiently high current gain ($h_{FEMIN} > 8$) and a base drive resistor low enough to ensure that the transistor easily saturates.

Table 1:
Recommended NPN Transistor

DEVICE	V_{CBO}	V_{CE0}	I_c	h_{FEMIN}	PACKAGE
MJE13002	600V	300V	1.5A	8	TO-126
MJE13003, KSE13003	700V	400V	1.5A	8	TO-126
STX13003	700V	400V	1A	8	TO-92

Figure 3:
Typical Application Circuit ($V_o=5V, I_o=500mA\sim 700mA$)



C1, C2	4.7 μ F/400V	Q1	'13002S, TO-92
C3	4.7nF/1kV	FR1	10
C4	4.7 μ F/25V	R2	300k
C5	680 μ F/10V	R3, R10	100,200
C6	1nF/50V	R4	33
C7	470pF/50V	R5	See Table 2
D1-D4	1N4007	R6	See Table 2
D5	FR107	R7, R8	1M
D6	HER103	R9	390
D7	1N4148	R11	1k
D8	SB240	R12	10
L1	2mH	T1	See Table 2

Design Procedure

Figure 3, *Typical Application Circuit*, shows a complete, optimized constant voltage/constant current charger application. The application design procedure for using the ACT355A is simple. Three components determine the output constant voltage

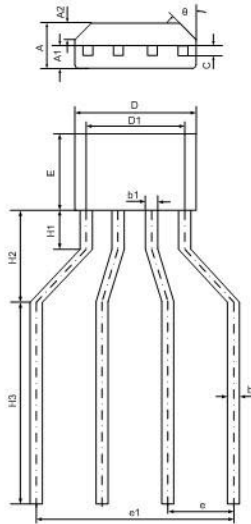
and constant current settings: the transformer T_1 and resistors R_5 and R_6 . Refer to Table 2 for selection values for these three key components for different typical design cases. The *Typical Application Circuit* in Figure 3 lists component values of other devices in the a complete charger application

Table 2:
Component Selection Table

DESIGN CASE	OUTPUT		ActivePSR™ PART NUMBER	TRANSFORMER				RESISTOR NETWORK	
	V _o (V)	I _o (mA)		N _P	N _A	N _S	L _P (mH)	R ₅ (kΩ)	R ₆ (kΩ)
1	5.0	500	ACT355A	130	32	10	1.5±7%	26.1	6.81
2	5.0	600	ACT355A	130	32	10	1.7±7%	30.1	8.06
3	5.0	650	ACT355A	130	32	10	1.8±7%	32.4	8.66
4	5.0	700	ACT355A	130	32	10	1.9±7%	35.7	9.31

PACKAGE OUTLINE

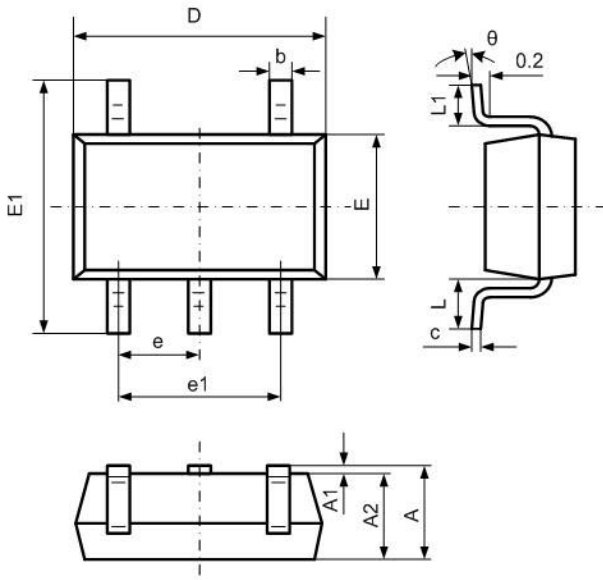
SIP-4 PACKAGE OUTLINE AND DIMENSIONS (AMMO TAPE PACKING)



SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	1.400	1.800	0.055	0.071
A1	0.700	0.900	0.028	0.035
A2	0.500	0.700	0.020	0.028
b	0.360	0.500	0.014	0.020
b1	0.380	0.550	0.015	0.022
C	0.360	0.510	0.014	0.020
D	4.980	5.280	0.196	0.208
D1	3.780	4.080	0.149	0.161
E	3.450	3.750	0.136	0.148
e	2.200	2.800	0.086	0.110
e1	6.600	8.400	0.259	0.330
H1	1.350	1.650	0.053	0.065
H2	3.370	3.670	0.133	0.144
H3	10.83	11.13	0.426	0.438
θ	45° TYP		45° TYP	

PACKAGE OUTLINE

SOT23-5 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.700 REF		0.028 REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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