KA3882C/KA3883C

SMPS Controller

Features

- Low Start Current 0.2mA (Typ)
- Operating Range Up To 500kHz
- Cycle by Cycle Current Limiting
- Under Voltage Lock Out With Hysteresis
- Short Shutdown Delay Time: Typ.100ns
- High Current Totem-Pole Output
- Output Swing Limiting: 22V

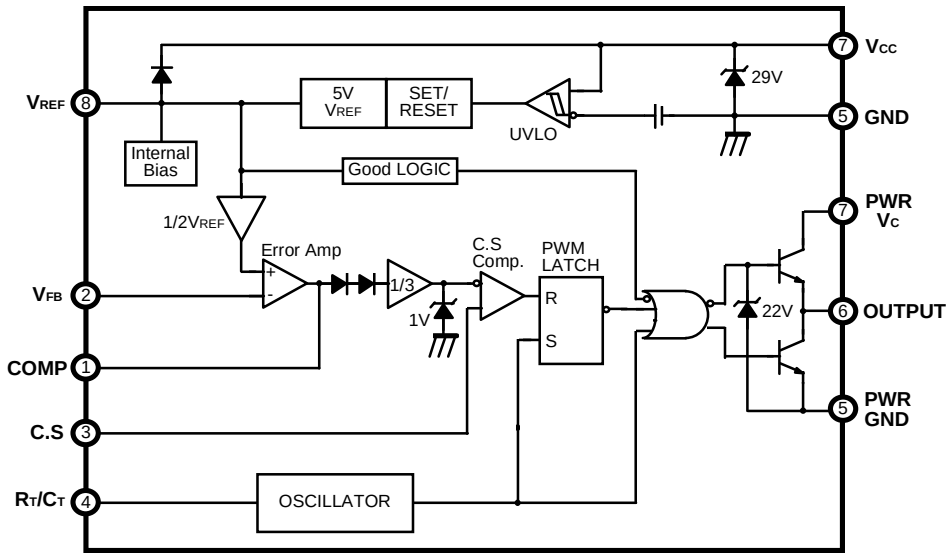
Description

The KA3882C/KA3883C is a fixed PWM controller for Off Line and DC to DC converter applications. The internal circuits include an UVLO, a low start up current circuit, a temperature compensated reference, a high gain error amplifier, a current sensing comparator, and the high current totem-pole output for driving a POWER MOSFET. Also the KA3882C/KA3883C provides low start-up current below 0.3mA and short shutdown delay time typ. 100ns. The KA3882C has the UVLO threshold of 16V (on) and 10V(off). The KA3883C is 8.4V(on) and 7.6V(off). The KA3882C and KA3883C can operate within 100% duty cycle.

8-DIP

8-SOP

Internal Block Diagram



Rev. 1.0.1

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	30	V
Output Current	I_O	±1	A
Analog Inputs (pin 2, 3)	$V_{I(ANA)}$	-0.3 to 6.3	V
Error Amp. Output Sink Current	$I_{SINK(EA)}$	10	mA
Power Dissipation	P_D	1	W
Thermal Resistance, Junction-to-Air (Note4) 8-SOP 8-DIP	$R\theta ja$	 280 95	°C/W
Storage Temperature	T_{stg}	-65 ~ 150	°C

Electrical Characteristics

(V_{CC} = 15V, R_T = 10kΩ, C_T = 3.3nF, T_A = 0°C to +70°C ,Unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
REFERENCE SECTION						
Output Voltage	V_{REF}	T_J = 25°C, I_O = 1mA	4.9	5.0	5.1	V
Line Regulation	ΔV_{REF}	V_{CC} = 12V to 25V	-	6	20	mV
Load Regulation	ΔV_{REF}	I_O = 1mA to 20mA	-	6	25	mV
Output Short Circuit	I_{SC}	T_a = 25°C	-	-100	-180	mA
OSILLATOR SECTION						
Initial Accuracy	F_{OSC}	T_J = 25°C	47	52	57	kHz
Voltage Stability	ST_V	V_{CC} = 12V to 25V	-	0.2	1	%
Amplitude	V_{OSC}	V_{PIN4}, Peak to Peak	-	1.7	-	V
Discharge Current	I_{DISCHG}	T_J = 25°C, Pin4 = 2V	7.8	8.3	8.8	mA
CURRENT SENSE SECTION						
Gain	G_V	(Note2, 3)	2.85	3	3.15	V/V
Maximum Input Signal	$V_{I(MAX)}$	V_{PIN1} = 5V(Note2)	0.9	1.0	1.1	V
PSRR	PSRR	V_{CC} = 12V to 25V (Note1, 2)	-	70	-	dB
Input Bias Current	I_{BIAS}	-	-	-2	-10	uA
Delay to Output	T_D	V_{PIN3} = 0 V to 2V (Note1)	-	100	200	ns

Electrical Characteristics (Continued)

(V_{CC} = 15V, R_T = 10kΩ, C_T = 3.3nF, T_A = 0°C to +70°C, Unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
ERROR AMPLIFIER SECTION						
Input Voltage	V_I	T_{PIN1} = 2.5V	2.42	2.50	2.58	V
Input Bias Current	I_{BIAS}	-	-	-0.3	-2	uA
Open Loop Gain	G_{VO}	V_O = 2V to 4V (Note1)	65	90	-	dB
Unity Gain Bandwidth	GBW	T_J= 25°C (Note1)	0.7	1	-	MHz
PSRR	PSRR	V_{CC} = 12V to 25V (Note1)	60	70	-	dB
Output Sink Current	I_{SINK}	V_{PIN2} = 2.7V, V_{PIN1} = 1.1V	2	6	-	mA
Output Source Current	I_{SOURCE}	V_{PIN2} = 2.3V, V_{PIN1} = 5.0V	-0.5	-0.8	-	mA
Output High Voltage	V_{OH}	V_{PIN2} = 2.3V, R1 = 15kΩ to GND	5	6	-	V
Output Low Voltage	V_{OL}	V_{PIN2} = 2.7V, R1 = 15kΩ to Pin8	-	0.8	1.1	V
OUTPUT SECTION						
Output Low Level	V_{OL}	I_{SINK} = 20mA	-	0.1	0.4	V
		I_{SINK} = 200mA	-	1.5	2.2	V
Output High Level	V_{OH}	I_{SOURCE} = 20mA	13	13.5	-	V
		I_{SOURCE} = 200mA	12	13.5	-	V
Rise Time	t_R	T_J = 25°C, C1 = 1nF (Note1)	-	40	100	ns
Fall Time	t_F	T_J = 25°C, C1 = 1nF (Note1)	-	40	100	ns
Output Voltage Swing Limit	V_{OLIM}	V_{CC} = 27V, C1 = 1nF	-	22	-	V
UNDER VOLTAGE LOCKOUT SECTION						
Start Threshold	V_{TH}	KA3882C	15	16	17	V
		KA3883C	7.8	8.4	9.0	V
Min. Operating Voltage (After turn on)	V_{TL}	KA3882C	9	10	11	V
		KA3883C	7.0	7.6	8.2	V
PWM SECTION						
Maximum Duty Cycle	D_{MAX}	KA3882C/KA3883C	94	96	100	%
Minimum Duty Cycle	D_{MIN}	-	-	-	0	%
TOTAL STANDBY CURRENT						
Start-Up Current	I_{ST}	-	-	0.2	0.4	mA
Operating Supply Current	I_{CC}	V_{PIN2} = V_{PIN3} = 0V	-	11	17	mA
V_{CC} Zener Voltage	V_Z	I_{CC} = 25mA	-	29	-	V

* Adjust V_{CC} above the start threshold before setting at 15V

Notes :

1. These parameters, although guaranteed, are not 100% tested in production.
2. Parameter measured at trip point of latch with V2 = 0V.
3. Gain defined as: $G_V = \Delta V_{PIN1} \Delta V_{PIN3} (V_{PIN3}$ = 0 to 0.8V)
4. Junction-to-air thermal resistance test enviroments.

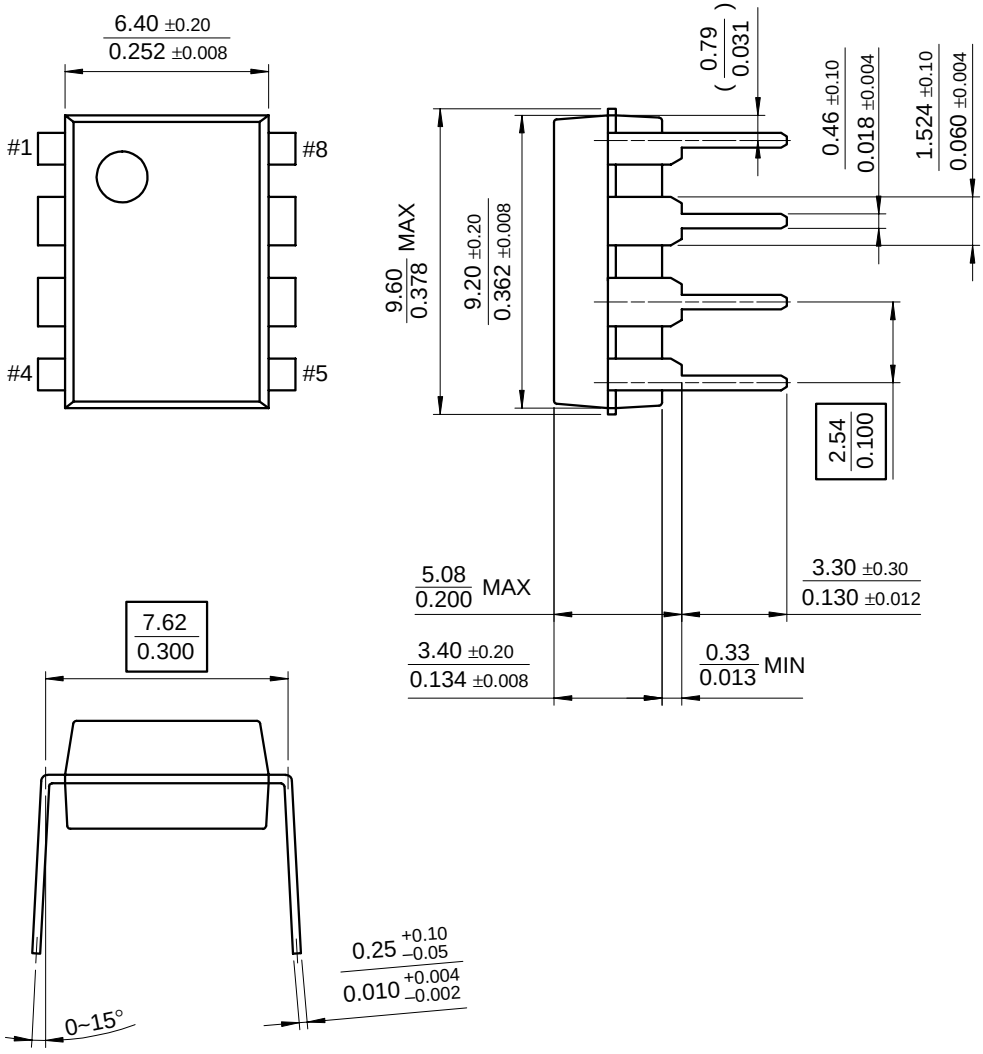
-. PCB information ;
Board thickness : 1.6mm , Board dimension : 76.2 X 114.3mm^2 , Ref. : EIA / JSED51-3 and EIA / JSED51-7

-. Board structure; Using the single layer PCB.

Mechanical Dimensions

Package

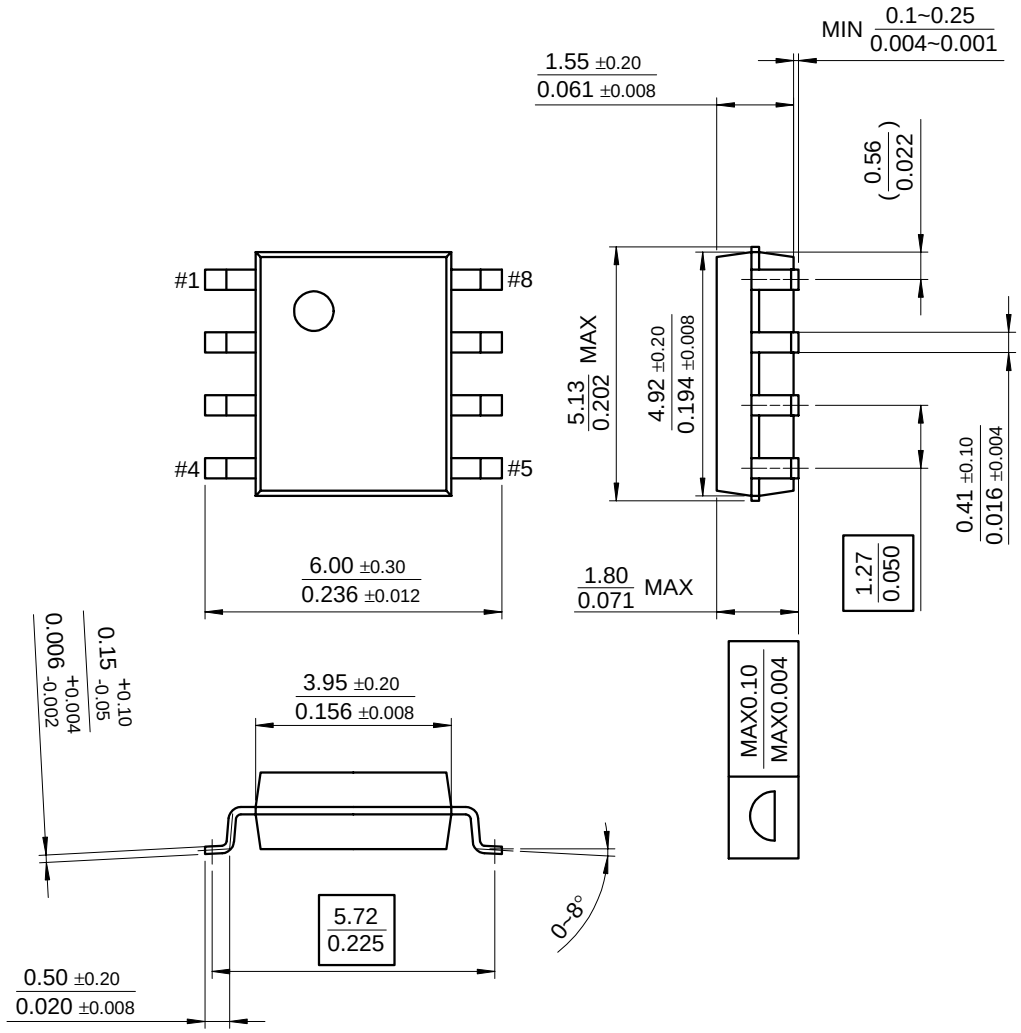
8-DIP



Mechanical Dimensions (Continued)

Package

8-SOP



Ordering Information

Product Number	Package	Operating Temperature
KA3882C	8-DIP	0 ~ +70°C
KA3882CD	8-SOP	
KA3883C	8-DIP	
KA3883CD	8-SOP	