■ Description

The FA1384X series are CMOS current mode control ICs for off-line and DC-to-DC converters.
These ICs can reduce start-up circuit loss and are optimum for high efficiency power supplies because of the low power dissipation achieved through changes in the CMOS fabrication process.
These ICs can drive a power MOSFET directly.
The high-performance, compact power supply can be designed with minimal external components .

■ Features

- CMOS process
- Low-power dissipation
- Standby current 2μA (max.), start-up current 30μA (max.)
- Pulse-by-pulse current limiting
- 5V bandgap reference
- UVLO (Undervoltage lockout) with hysteresis
- Maximum duty cycle FA13842, 13843: 96%
  FA13844, 13845: 48%
- Pin-for-pin compatible with UC384X

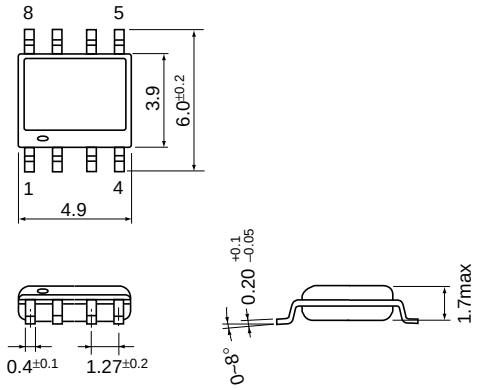
Note: *Pins are fully compatible, but characteristics are not. When our ICs are applied to a power supply circuit designed for other manufactures' 384X series, the characteristics and safety features of the power supply must be checked.*

■ Types of FA1384X series

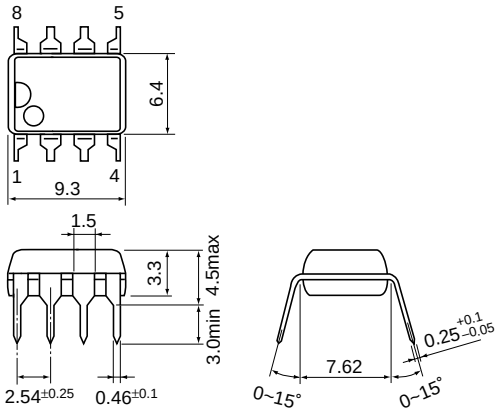
Type	UVLO		Maximum duty cycle	Package
	Start threshold	Stop threshold		
FA13842P	16.5V±1V	9V±1V	96%	DIP
FA13842N				SOP
FA13843P	9.6V±1V	9V±1V	96%	DIP
FA13843N				SOP
FA13844P	16.5V±1V	9V±1V	48%	DIP
FA13844N				SOP
FA13845P	9.6V±1V	9V±1V	48%	DIP
FA13845N				SOP

■ Dimensions, mm

● SOP-8

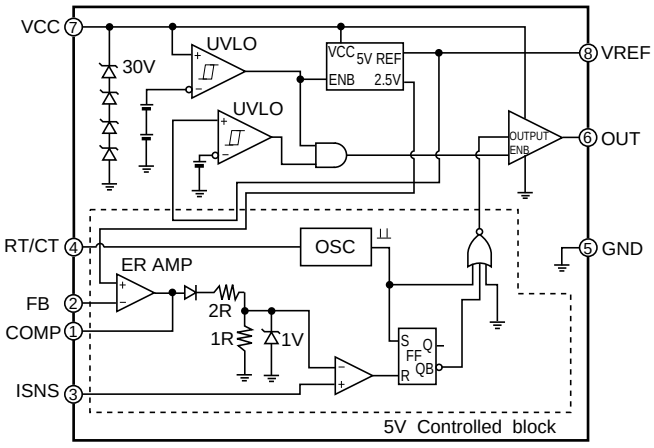


● DIP-8

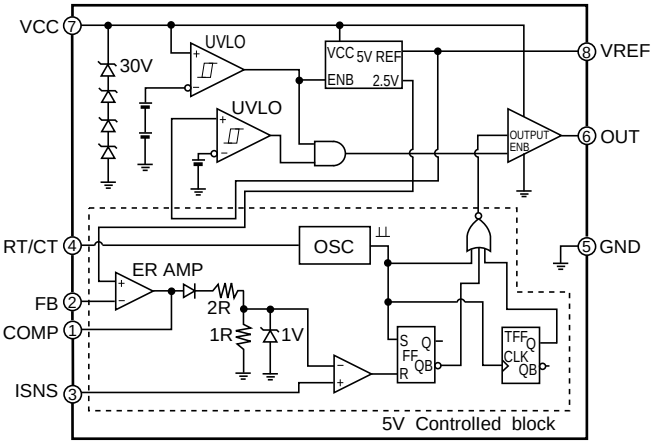


■ Block diagram

● **FA13842, 13843**



● **FA13844, 13845**



Pin No.	Symbol	Function	Description
1	COMP	Compensating	Error amplifier output, available for loop compensation circuit
2	FB	Feedback	Inverting input of the error amplifier
3	ISNS	Current sensing	Input voltage proportional to inductor current
4	RT/CT	Oscillator control	Setting oscillation frequency and maximum duty-cycle with resistor R_T and capacitor C_T
5	GND	Ground	Ground
6	OUT	Output	Output for driving a power MOSFET
7	VCC	Power supply	Power supply
8	VREF	Reference voltage	Reference voltage and current source charging capacitor C_T through resistor R_T

■ Absolute maximum ratings (Ta=25˚C)

Item	Symbol	Test condition		Rating	Unit
Supply voltage	V_{CC}	Low impedance source		28	V
		Zener clamp (Icc<10mA)		Self limiting	V
Zener current	I_Z			10	mA
Output peak current	I_O	Source current		400	mA
		Sink current		1	A
FB/ISNS terminal input voltage	V_{IN}	FB, ISNS		–0.3 to 5.3	V
Error amplifier sink current	I_{SINK}			10	mA
Total power dissipation	P_d	at Ta < 50˚C	DIP	800	mW
			SOP	400	
Thermal resistance	$R_{\theta j\text{-}a}$	Junction-air	DIP	125	˚C/W
			SOP	250	
Junction temperature	T_j			150	˚C
Ambient temperature	T_a			–25 to 85	˚C
Storage temperature	T_{stg}			–40 to 150	˚C

■ Recommended operating conditions

Item	Symbol	Min.	Max.	Unit
Supply voltage	V_{CC}	10	25	V
Oscillation timing capacitor	C_T	0.47	10	nF
Oscillation timing resistor	R_T	2.0	100	kΩ
Oscillation frequency	f_{OSC}	10	500	kHz

■ Electrical characteristics (Vcc=15V, R_T=10kΩ, C_T=3.3nF, Ta=25˚C)

Reference voltage section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Reference voltage	V_{REF}	Tj=25˚C, I_L=1mA	4.75	5.00	5.25	V
Line regulation	L_{INE}	Vcc=10 to 25V		±3	±20	mV
Load current regulation	L_{OAD}	I_L=0 to 20mA		±3	±25	mV
Temperature regulation	V_{TC}	Ta=–25 to 85˚C		±0.3		mV/˚C
Output current at short-circuit	I_{OS}	Tj=25˚C		60		mA

Oscillator section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC}	Tj=25˚C	49	52	55	kHz
		Ta=–25 to 85˚C	47		57	kHz
Voltage stability	fdv	Vcc=10 to 25V		±0.25	±1	%
Temperature stability	fdt	Ta=–25 to 85˚C		–0.07		%/˚C
Oscillation amplitude	V_{OSC}	Tj=25˚C		1.6		V
Discharge current	I_{DISCHG}	Tj=25˚C		8.4		mA

Error amplifier section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input voltage	V_{FB}	COMP=2.5V, Tj=25˚C	2.4	2.5	2.6	V
Input leak current	I_{FB}				±2	µA
Open-loop gain	A_V		65	72		dB
Unity gain bandwidth	f_T		0.7	1		MHz
Output source current	I_{SOURCE}	FB=2.3V, COMP=0V	–0.8	–1.0		mA
Output sink current	I_{SINK}	FB=2.7V, COMP=1V	2	15		mA
Output voltage	$V_{H\ COMP}$	FB=2.3V, R_L=15kΩ to GND	4.0	4.5		V
	$V_{L\ COMP}$	FB=2.7V, R_L=15kΩ to VREF		80	500	mV

Current sensing section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Voltage gain	$A_{V\ IS}$	Tj=25˚C	2.85	3	3.15	V/V
Maximum input signal	$V_{TH\ IS}$	FB=0V	0.9	1.0	1.1	V
Input bias current	I_{IS}			–1	–5	µA
Delay to output	T_{PD}	Tj=25˚C, ISNS to OUT		150	300	ns

Output section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
High-level output	V_{OH}	I source=–20mA	14.5	14.75		V
		I source=–100mA	12	13.5		V
Low-level output	V_{OL}	I sink=20mA		0.15	0.3	V
		I sink=200mA		1.5	3	V
Rise time	tr	C_L=1nF, Tj=25˚C		40	150	ns
Fall time	tf	C_L=1nF, Tj=25˚C		20	150	ns

Under-voltage lockout section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Start threshold	$V_{TH\ ON}$	FA13842, 13844	15.5	16.5	17.5	V
		FA13843, 13845	8.6	9.6	10.6	V
Min. operating voltage	$V_{TH\ OFF}$		8	9	10	V
Hysteresis	V_{HYS}	FA13842, 13844		7.5		V
		FA13843, 13845		0.6		V

PWM section

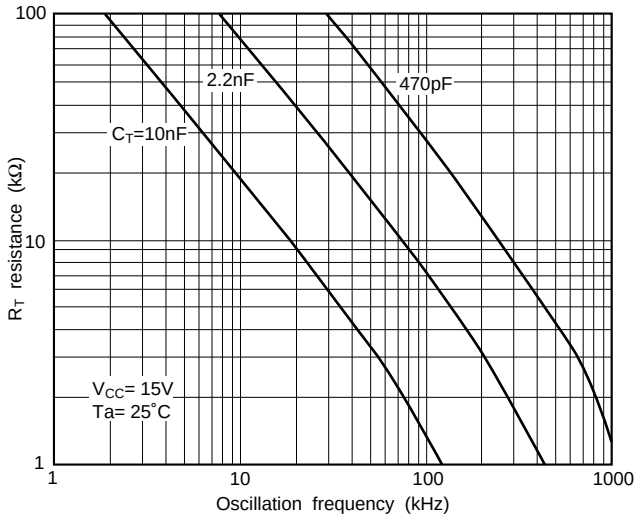
Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Maximum duty cycle	Dmax	FA13842, 13843	94	96	98	%
		FA13844, 13845	47	48	50	%
Minimum duty cycle	Dmin	FB=5V, COMP=Open			0	%

Overall device

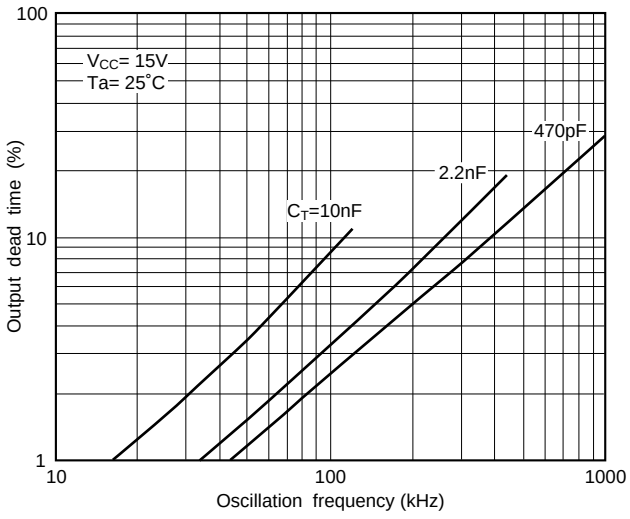
Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Standby current	I_{CCL}	FA13842, 13844 Vcc=14V			2	µA
		FA13843, 13845 Vcc=7V			2	µA
Start-up current	$I_{CC\ ST}$	Vcc=Start threshold		12	30	µA
Operating current	$I_{CC\ OP}$			3	5	mA
Zener voltage (Vcc)	V_Z	Icc=5mA	28	30	34	V

■ Characteristic curves (Ta=25˚C)

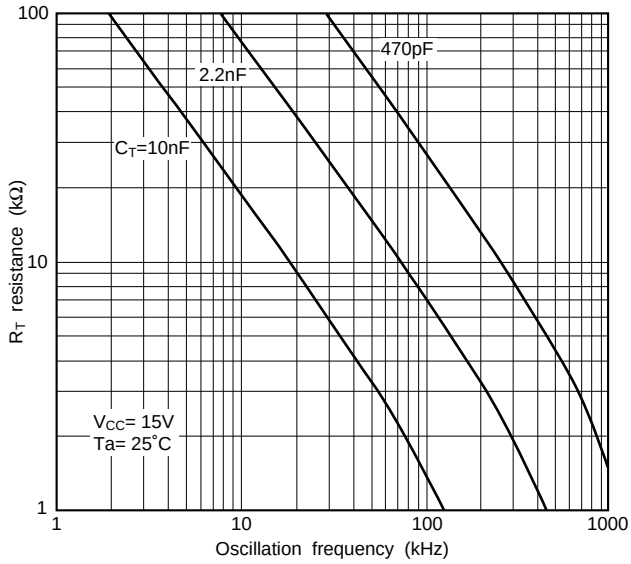
Timing resistance vs. oscillation frequency
FA13842, FA13843



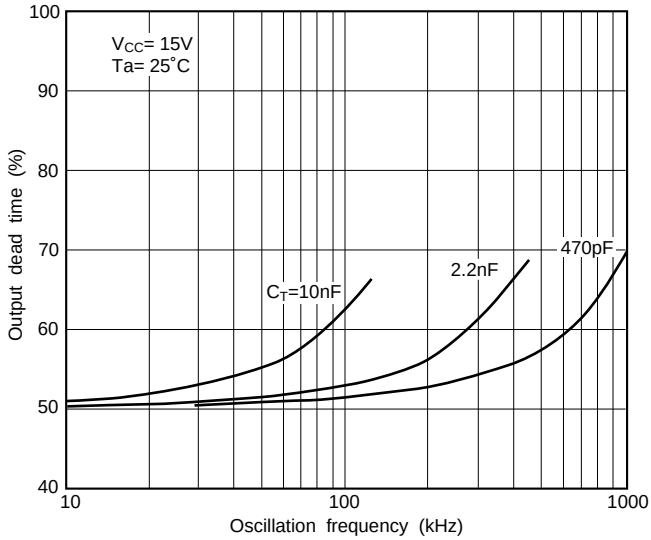
Output dead time vs. oscillation frequency
FA13842, FA13843



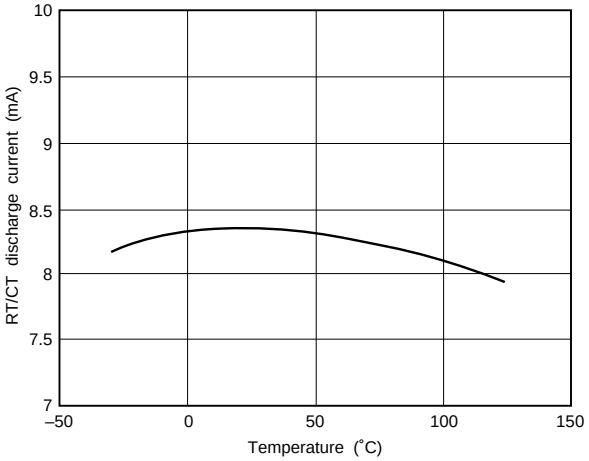
Timing resistance vs. oscillation frequency
FA13844, FA13845



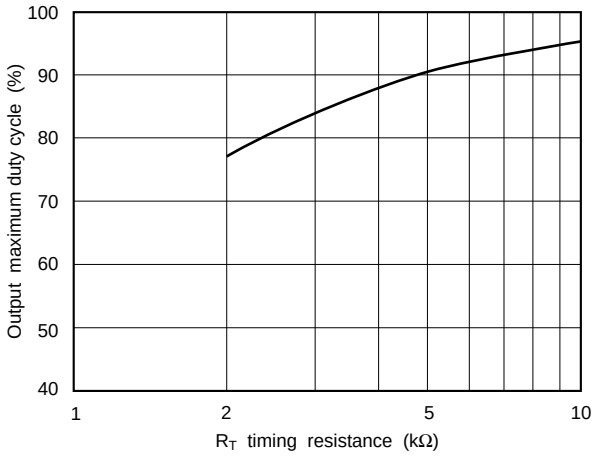
Output dead time vs. oscillation frequency
FA13844, FA13845



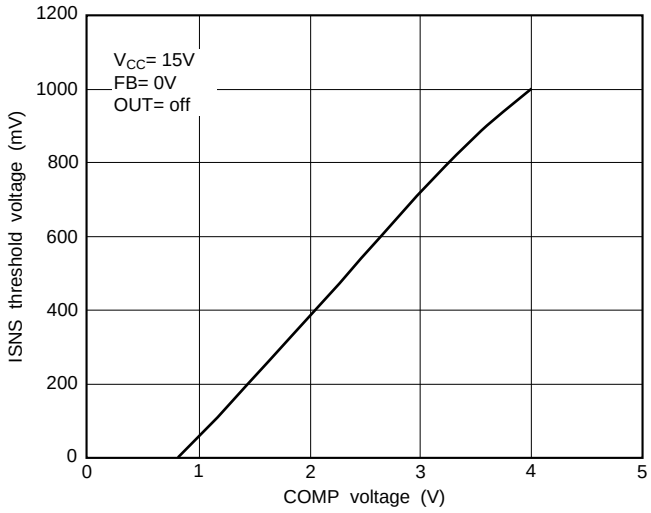
RT/CT discharge current vs. temperature



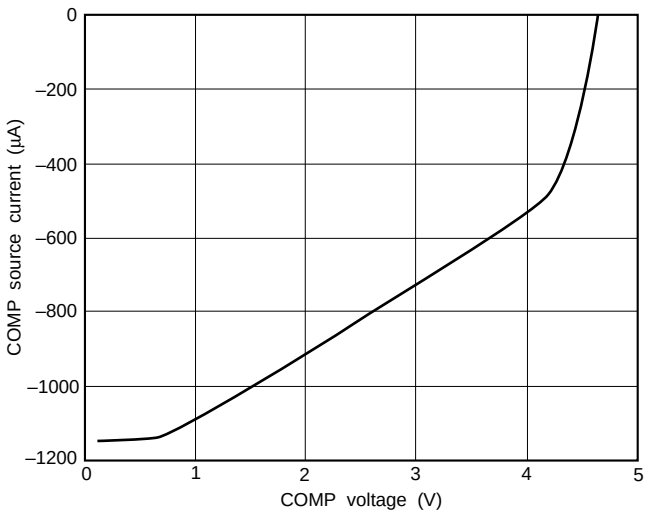
Output max. duty cycle vs. timing resistance
FA13842, FA13843



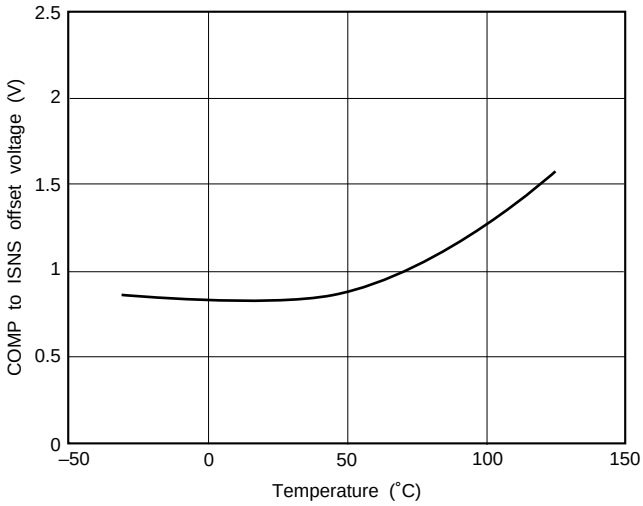
ISNS threshold voltage vs. COMP voltage



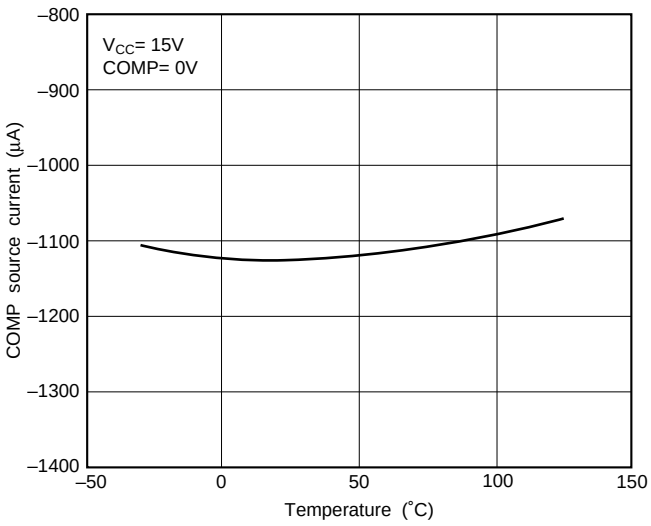
COMP source current vs. COMP voltage



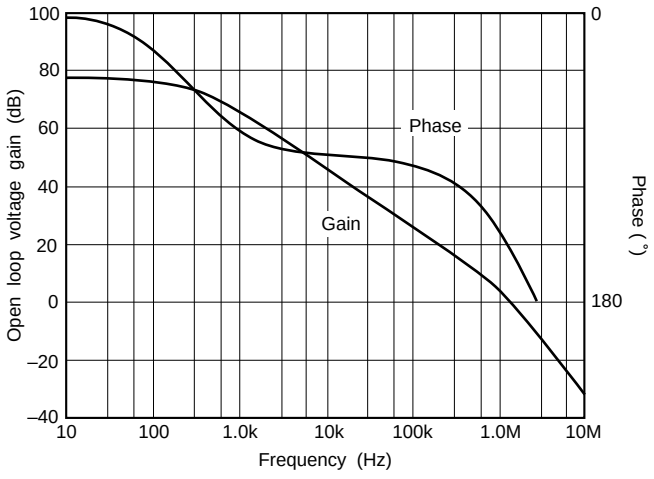
COMP to ISNS offset voltage vs. temperature



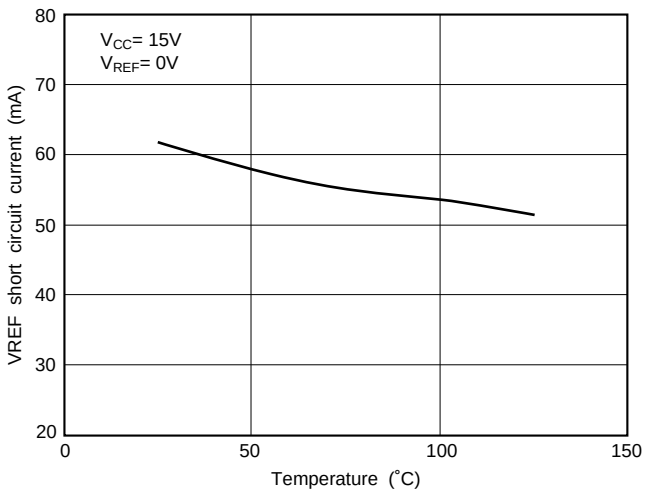
COMP source current vs. temperature



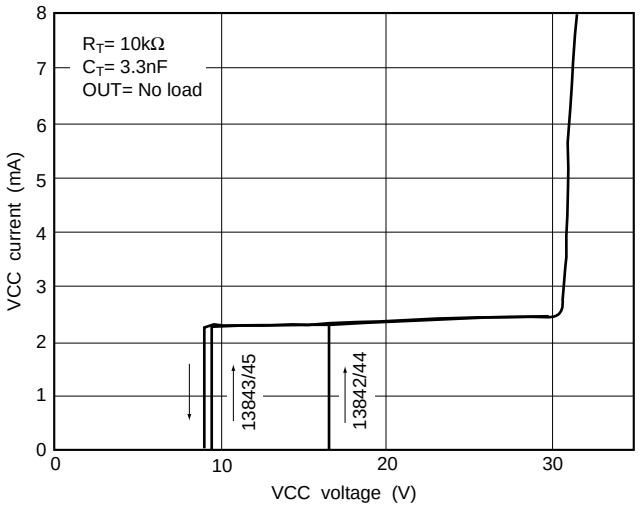
Error amp open loop voltage gain and phase vs. frequency



VREF short circuit current vs. temperature

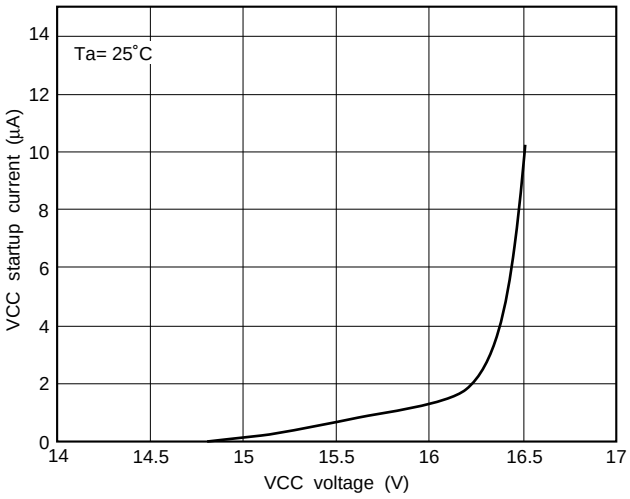


VCC supply current vs. VCC supply voltage



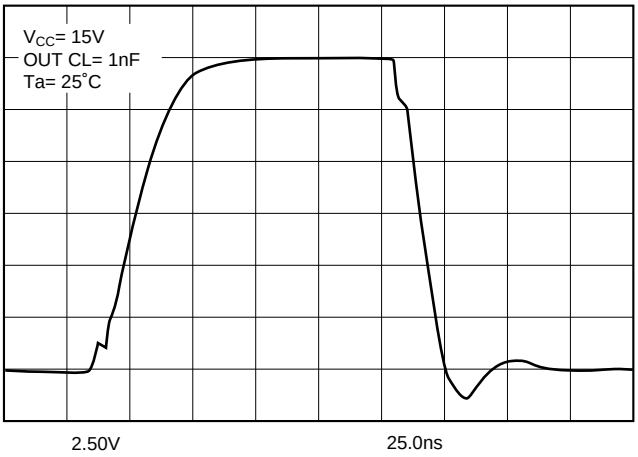
VCC startup current vs. VCC supply voltage

FA13842, FA13844

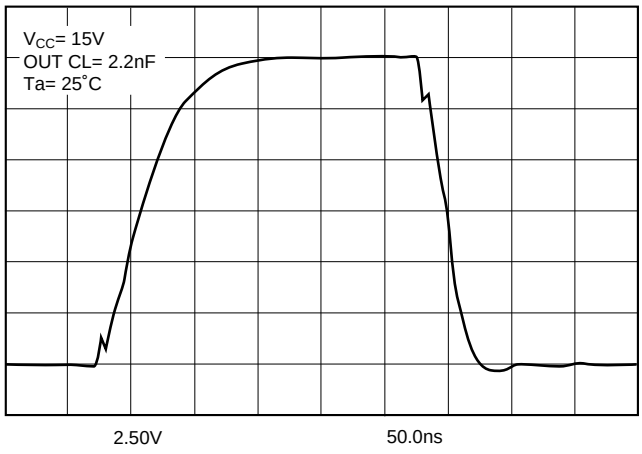


Output waveform

Vcc=15V, OUT CL=1nF, Ta=25˚C



Vcc=15V, OUT CL=2.2nF, Ta=25˚C



■ Description of each circuit

1. Oscillator

The oscillation frequency is determined by timing resistance R_T and timing capacitor C_T, which are connected to RT/CT terminal. C_T is charged to about 3V through R_T from a 5V reference, and discharged to about 1.4V by the built-in discharge circuit. (See Fig. 1, 2, 3.)
Blanking pulses are generated in the IC during the C_T discharge period.
The output is fixed in the "low" state by these pulses, and a fixed dead time is produced. See the characteristic curves on page 45 for the oscillation frequency, R_T and C_T.
In the case of FA13844/45, a flip-flop causes the output to be blanked with every other cycle. Therefore, the switching frequency of a power MOSFET is 1/2 of the oscillation frequency determined by R_T and C_T. (See Fig. 3.)

2. Error amplifier

Inverting input and output are connected to the FB terminal and COMP terminal, respectively. A 2.5V reference is connected internally to the non-inverting input.
The output voltage is offset by a diode V_F voltage (=0.7V) and divided by three. The divided voltage is connected to the input of the current sensing comparator.

3. Current sensing comparator and PWM latch

The "High" state of the OUT terminal begins at the time C_T starts charging. The OUT terminal turns to "Low" when the peak inductor current reaches the threshold level controlled by the error amplifier output (COMP terminal).
The inductor current is converted to a voltage by sensing resistor R_S inserted between GND and the source of a power MOSFET. This voltage is monitored by the ISNS terminal.

The peak current of inductor "Ipk" is expressed as follows:
$Ipk=(Vcomp-0.7) / (3 \bullet R_S)$ $0.7V \fallingdotseq V_F$
Vcomp: a voltage on COMP terminal

The maximum value of the threshold level of the current sensing comparator is held to 1V. Therefore, the maximum peak current "Ipk(max)" is as follows:
$Ipk(max)=1.0V/R_S$

4. Undervoltage lockout (UVLO)

In order to set the IC in the operation mode before the output stage(OUT terminal) is enabled, two under-voltage lockout comparators are incorporated to monitor the power supply voltage (V_{CC}) and reference voltage (V_{REF}).
The threshold level of the V_{CC} comparator is set at 16.5V/9V for FA13842/44 and 9.6V/9V for FA13843/45. In the standby mode, in which the V_{CC} is under ON threshold, the power supply current is maintained at nearly 0 (zero). However, a maximum current of 30μA is required to change from standby mode to operating mode .
The threshold level of the V_{REF} comparator is set at about 3.2V/2.0V.
A 30V zener diode is connected to V_{CC} and GND to protect the IC against overvoltages.

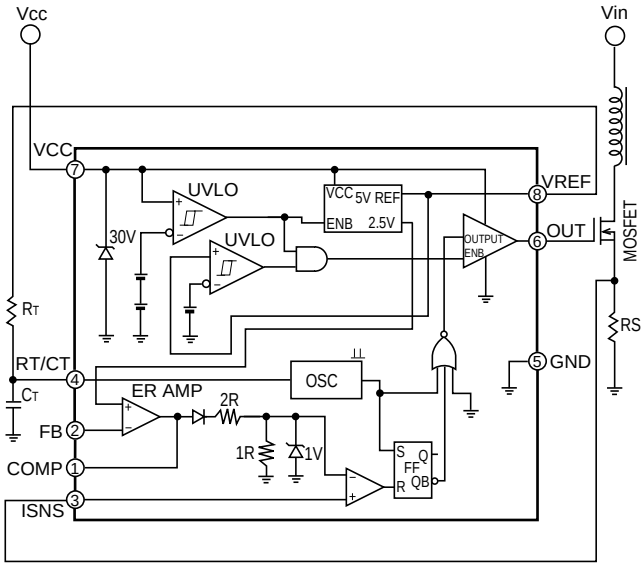


Fig. 1

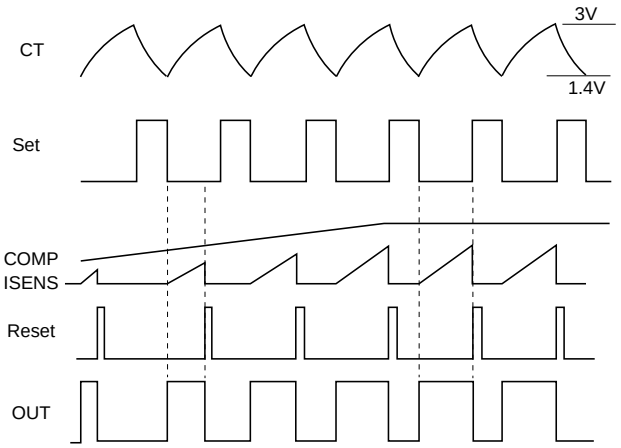


Fig. 2 FA13842, 13843

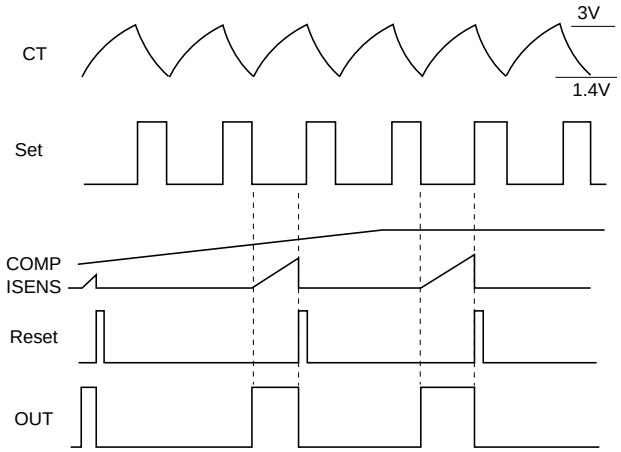


Fig. 3 FA13844, 13845

5. Output stage

An output stage of CMOS inverter composition is incorporated, thereby making it possible to fully swing the gate voltage of a power MOSFET to the V_{CC}.

The output stage provides a source current of 400mA and a sink current of 1A as the peak current capacity. (When V_{CC} is 15V)

The output stage is held in the "Low" state in standby mode.

6. Reference voltage

The 5.0V(±5%) bandgap reference(Tj=25˚C) is built-in.

It is possible to supply a current of about 10mA to an external circuit in addition to supplying a charge current to the timing capacitor of the oscillator. (See characteristic curve on page 46.)

Connect a ceramic bypass capacitor of 0.1µF or higher to the VREF terminal to stabilize this voltage.

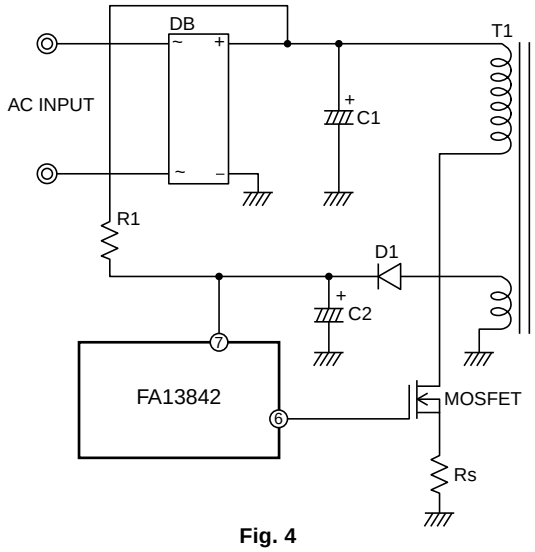


Fig. 4

■ Design advice

1. Start-up circuit

A typical start-up circuit is shown in Fig. 4.

The AC INPUT voltage charges capacitor C2 and supplies start-up current to the IC through start-up resistance R1. When this voltage reaches the ON threshold voltage, the IC reverts to the operation mode and electric power is supplied from the bias winding of the transformer thereafter.

Using CMOS process, the start-up current is less than 30µA.

When the start-up resistance is increased, the charging rate of capacitor C2 decreases and start-up time increases. Select the optimum values for R1 and C2.

The relation between the start-up resistance and start-up time for the circuit indicated in Fig. 4 is shown in Fig. 5.

Fig. 6 indicates a method to increase the start-up resistance to reduce loss and shorten start-up time. The start-up time is shortened by reducing the capacitance of C2. The bias current is supplied from C3 after start-up.

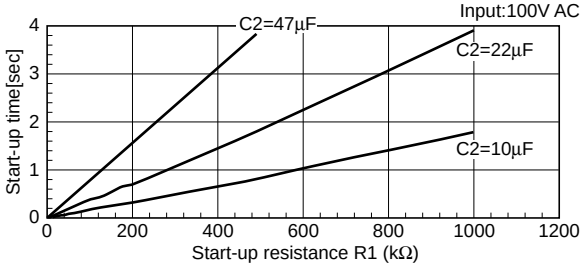


Fig. 5 Start-up time

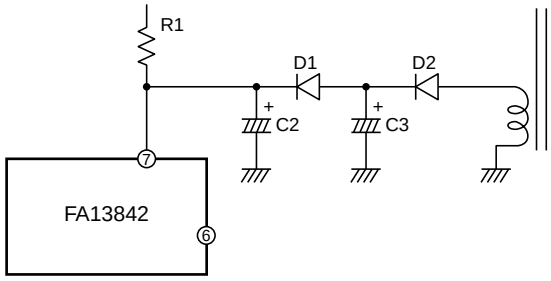


Fig. 6

2. Synchronized operation with external signals

The circuit shown in Fig. 7 allows synchronized operation with external signals.

Synchronized operation is started when the RT/CT terminal voltage is raised to about 3V or higher. (Synchronized at leading edge.)

The external synchronizing signal should be higher than the free-run frequency.

In the case of FA13844/45, the output frequency of the OUT terminal is 1/2 that of the synchronizing signal frequency.

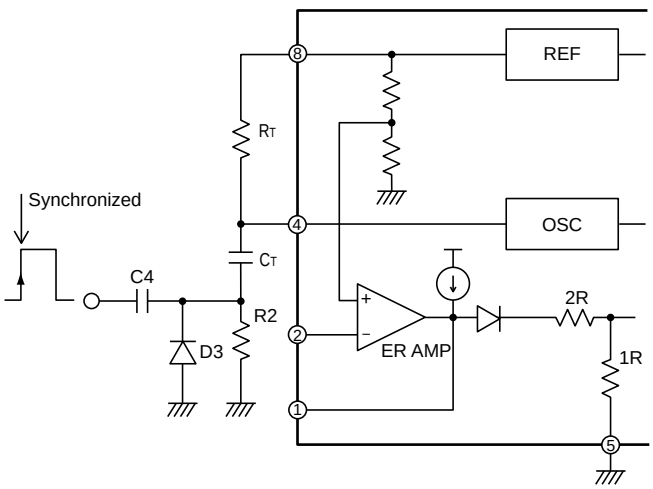


Fig. 7

3. Latched shutdown

A typical circuit for latched shutdown is shown in Fig. 8.
The voltage of the OUT terminal is kept low if the voltage of the COMP terminal is low. The voltage of the COMP terminal must be set at 0.7V or less in the application temperature range. (See characteristic curve on page 46 "COMP to ISNS offset voltage vs temperature".)
The source current from the COMP terminal is less than about 1.3mA.

Use of a thyristor such as that shown in Fig. 9 is not effective because the saturation voltage of the thyristor is higher than 0.7V. When a thyristor is used, increase the voltage of the FB terminal to more than 3V as shown in Fig.10. In the case of a latched shutdown, it is necessary to supply a current larger than the hold current of the thyristor structure circuit or of the thyristor. This current should be provided through a start-up resistor from the AC input.

Latched shutdown with a thyristor using the COMP terminal is not effective.

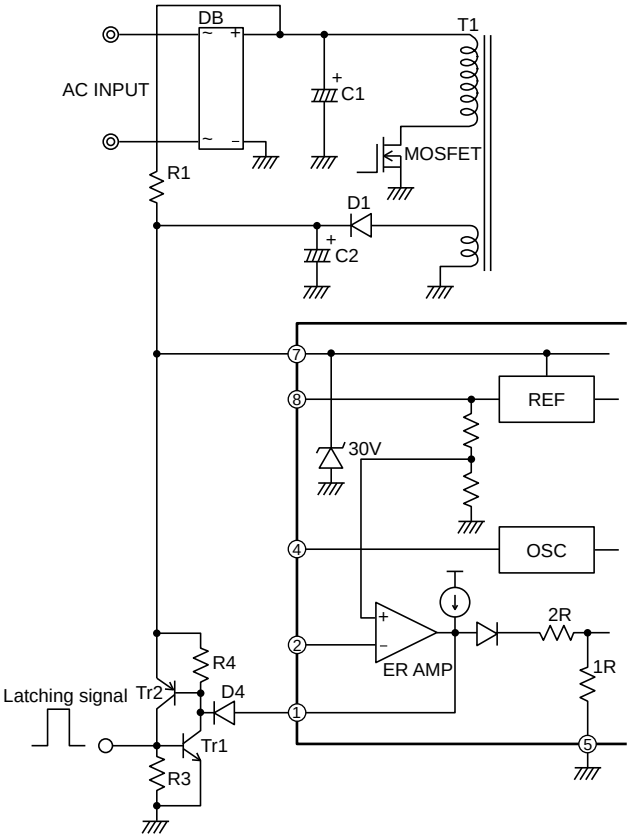


Fig. 8

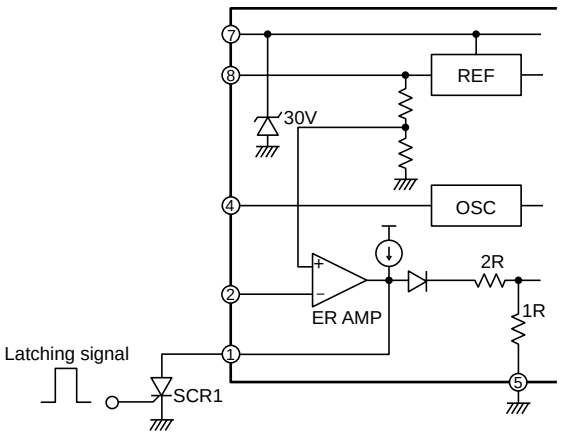


Fig. 9

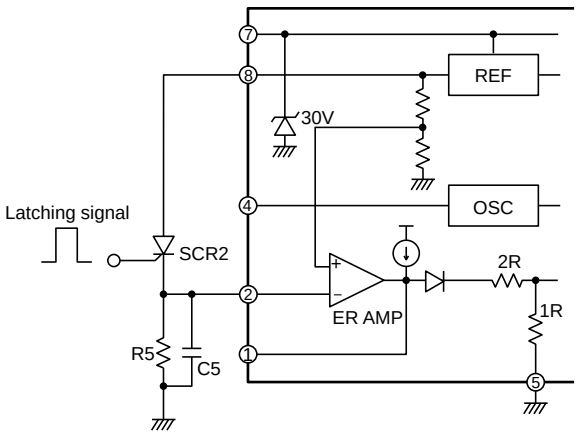


Fig. 10

3-1 The method of detecting an overvoltage (detection on primary side)

A typical latched shutdown circuit to protect against overvoltages detected on the primary side is shown in Fig. 11. When the secondary voltage increases in the flyback circuit, the voltage of the bias winding also increases in proportion. When this voltage increase is detected by zener diode ZD1, a latched shutdown is accomplished. As the secondary voltage is detected through a transformer, detection accuracy is low.

3-2 The method of detecting an overvoltage (detection on secondary side)

A typical latched shutdown circuit to protect against overvoltages detected on the secondary side is shown in Fig. 12.
The detected voltage accuracy is high compared to overvoltage detection on the primary side.

3-3 The method of detecting an overcurrent (detection of primary current)

A typical primary overcurrent detection circuit is shown in Fig. 13.

3-4 The method of detecting an overcurrent (detection of secondary current)

A typical secondary overcurrent detection circuit is shown in Fig. 14.

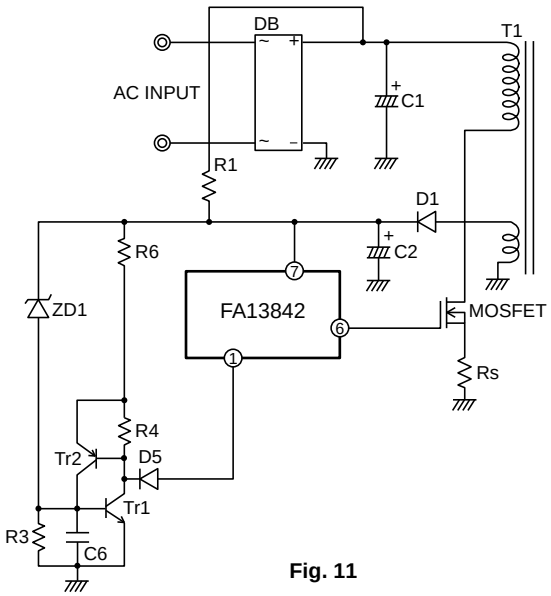


Fig. 11

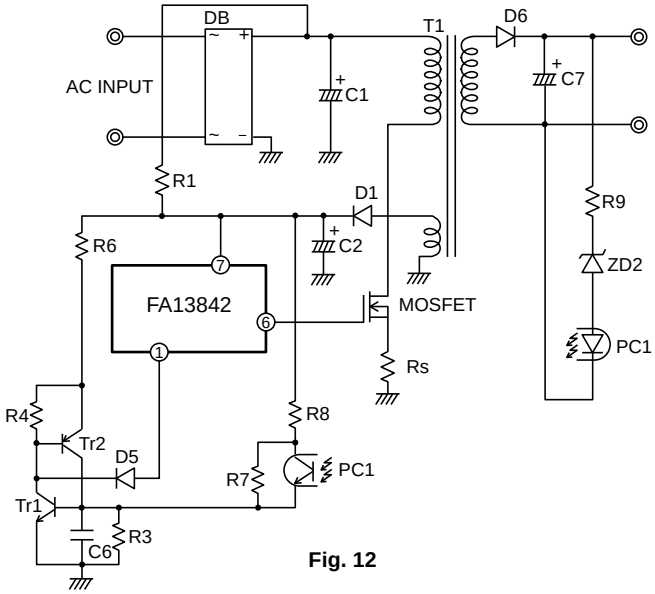


Fig. 12

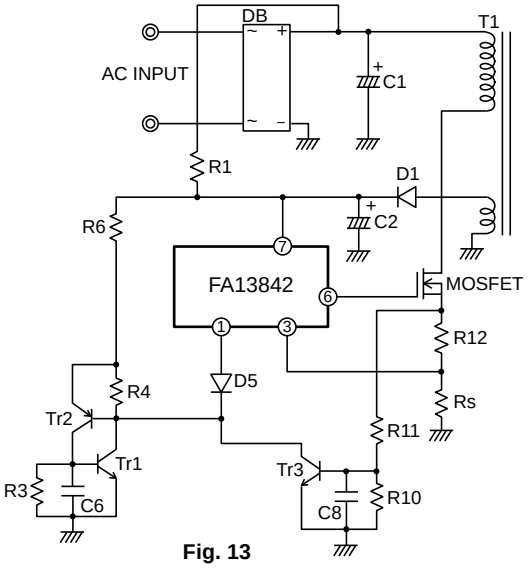


Fig. 13

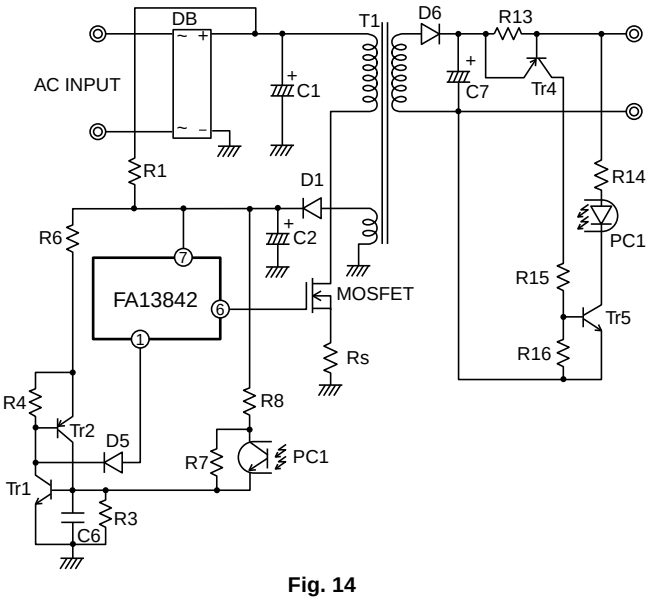


Fig. 14

4. Soft start

A soft-start circuit is shown in Fig. 15.
An aproximate soft-start time is determined with the following calculation. This soft-start time is defined as the time the ISNS terminal threshold voltage increases from 0V to 1V.

$t_{soft\text{-}start}$ [ms]=4.3•C9[μF]

5. Suppression of noise at the current sensing terminal

As each cycle current value is monitored in the current mode control, there is the possibility that a malfunction will occur even with a relatively low noise level. Therefore, it is necessary to add a CR filter to reduce the level of noise at the current sensing terminal. (See Fig. 16.)

6. ON/OFF circuit with an external signal

A typical ON/OFF circuit is shown in Fig. 17.
The output stage (OUT terminal) is enabled when the voltage at the FB terminal is reduced to less than 2.0V and is disabled when the FB terminal voltage increases to more than 3V.
Set the voltage of the FB terminal at a maximum of 5.3V in this case.

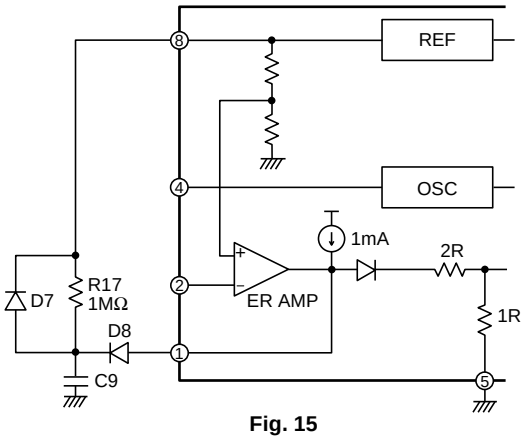


Fig. 15

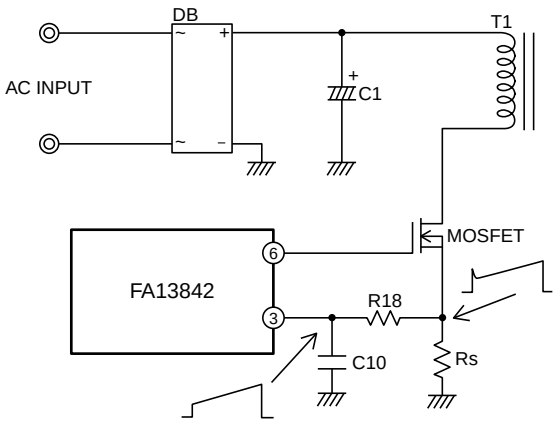


Fig. 16

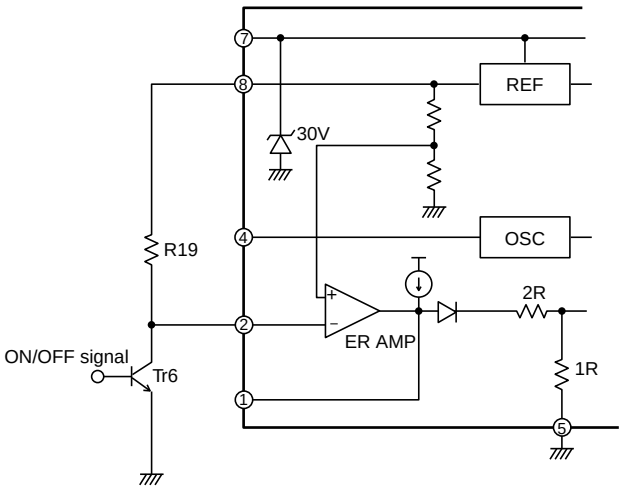


Fig. 17

7. Feedback circuit

7-1 A method that does not use an internal ER AMP

A method that does not use an internal ER AMP is shown in Fig. 18. Connect the FB terminal to GND and connect an optocoupler to the COMP terminal of the ER AMP output for feedback control.
It is possible to obtain a precise power supply output voltage, because the output voltage is monitored directly on the secondary side.
Be sure to connect the FB terminal to the GND in this case. There is the possibility of a malfunction occuring if the FB terminal is open.

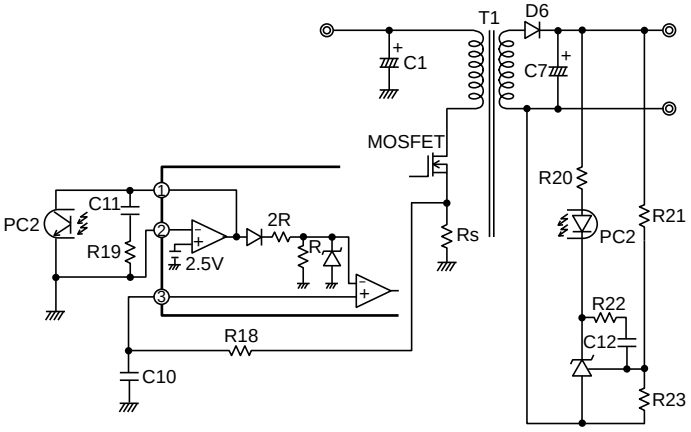


Fig. 18

7-2 A method using an internal ER AMP

A method using an internal ER AMP is shown in Fig. 19.
In the flyback circuit, the bias winding voltages of the transformer are proportional to the secondary winding voltage. Therefore, V_{CC} is approximately proportional to the DC output voltage on the secondary side.
V_{CC} is divided by resistors and monitored at the FB terminal to control the output voltage.
This feedback circuit consists of a minimal number of external components. However, regulation of the DC output voltage is poor because the output voltage is not monitored directly.

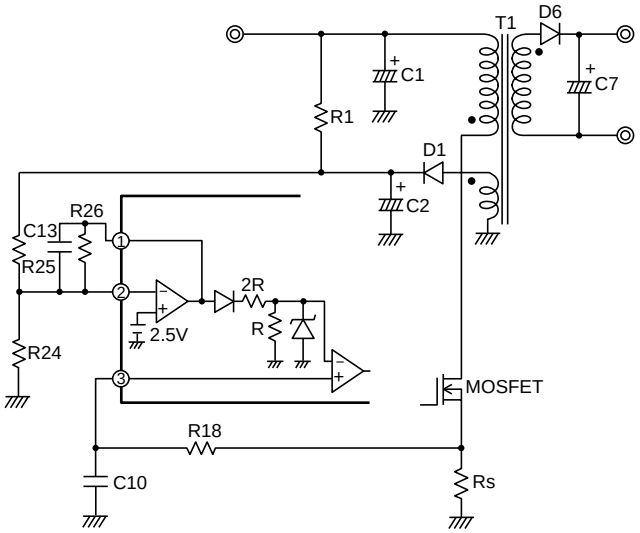


Fig.19

8. Slope compensation

It is well known that a current mode converter that controls peak current can oscillate irregularly when the inductor current is continuous and the duty cycle is greater than 50%.
This irregular oscillation is called subharmonic oscillation.
The period of subharmonic oscillation is equal to the integral number of the switching periods.
This phenomenon is shown in Fig. 20.
Lu indicates the positive slope of the inductor current. The slope is determined by the input voltage and the primary inductance value of the transformer. –Ld indicates the negative slope, which is determined by the rate of energy discharge to the secondary side.

Fig. 20 shows the inductor current waveform when T reveals the oscillation period and Is reveals the control signal of the peak inductor current. T_{ON} and T_{OFF} vary even when having the same T, Is, Lu and –Ld.
If it is assumed in Fig. 21 that the inductor current varies Δi_L at t0, the variation $\Delta i_L'$ of the inductor current at t1 is larger than Δi_L at t0. Thereafter, this inductor current variation gradually increases, and as a result, subharmonic oscillation occurs.

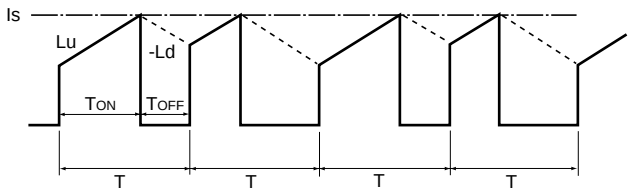


Fig. 20

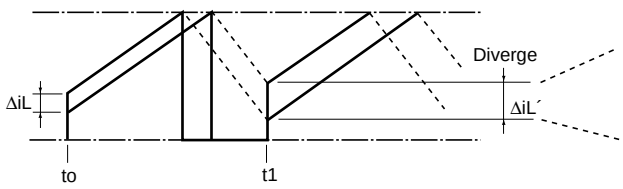


Fig. 21

Fig. 22 illustrates a case when the inductor current variation $\Delta i_L'$ at t1 is smaller than Δi_L at t0. In this case, inductor current variations gradually converges and the inductor current becomes stable.
It is necessary to apply slope compensation to the control signals in order to prevent such subharmonic oscillations when the inductor current is continuous and the duty cycle is greater than 50%.

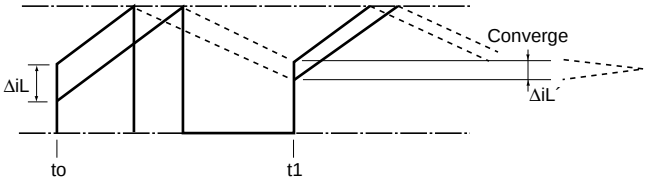


Fig. 22

The waveform of the inductor current when slope compensation is applied is shown in Fig. 23.
Slope compensation adds the negative slope of inclination –Kc to the control signal of the inductor peak current.
$\Delta i_L'$ shows the variation of the inductor current at t1 when slope compensation is not applied, and $\Delta i_L's$ shows the variation of the inductor current at t1 when slope compensation is applied.
Thus, $\Delta i_L'$ can be changed by –Kc, and $\Delta i_L's$ becomes smaller when –Kc is large. It is necessary to apply slope compensation to satisfy the equation $\Delta i_L \geq \Delta i_L's$, that is,
$|-Kc| \geq |-1/2\ Ld|$ as the condition which achieves stable operation.
Typical circuits are shown in Fig. 24 and 25.

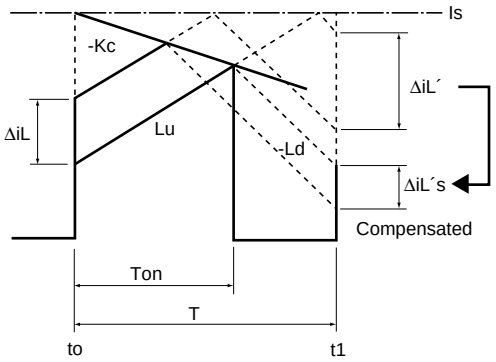


Fig. 23

9. Notice just before the IC is stopped
In some application, especially in the high frequency operation, the oscillator waveform is distorted just before the IC is stopped by UVLO.
It is supposed that this distortion does not cause a abnormal output pulse because the current sense compalator is enable. However, in the case of high frequency operation (more than 300kHz), check the operation just before the IC is stopped.

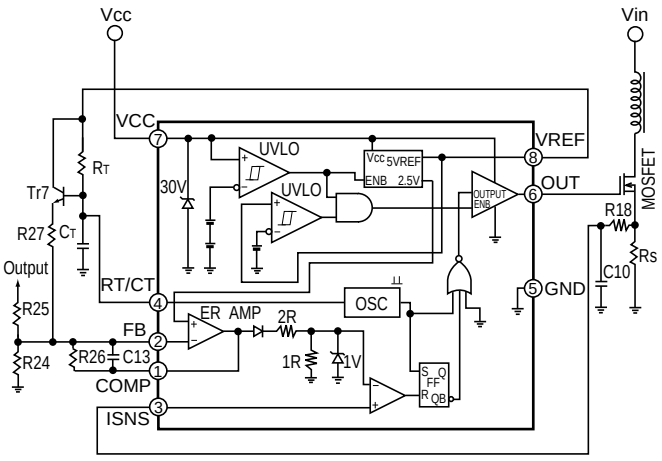


Fig. 24

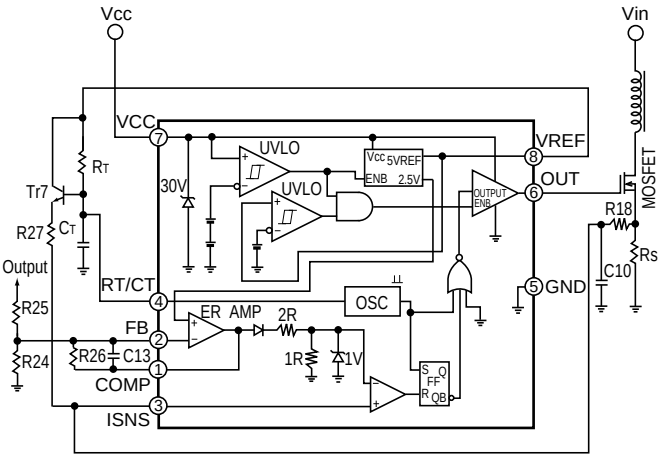
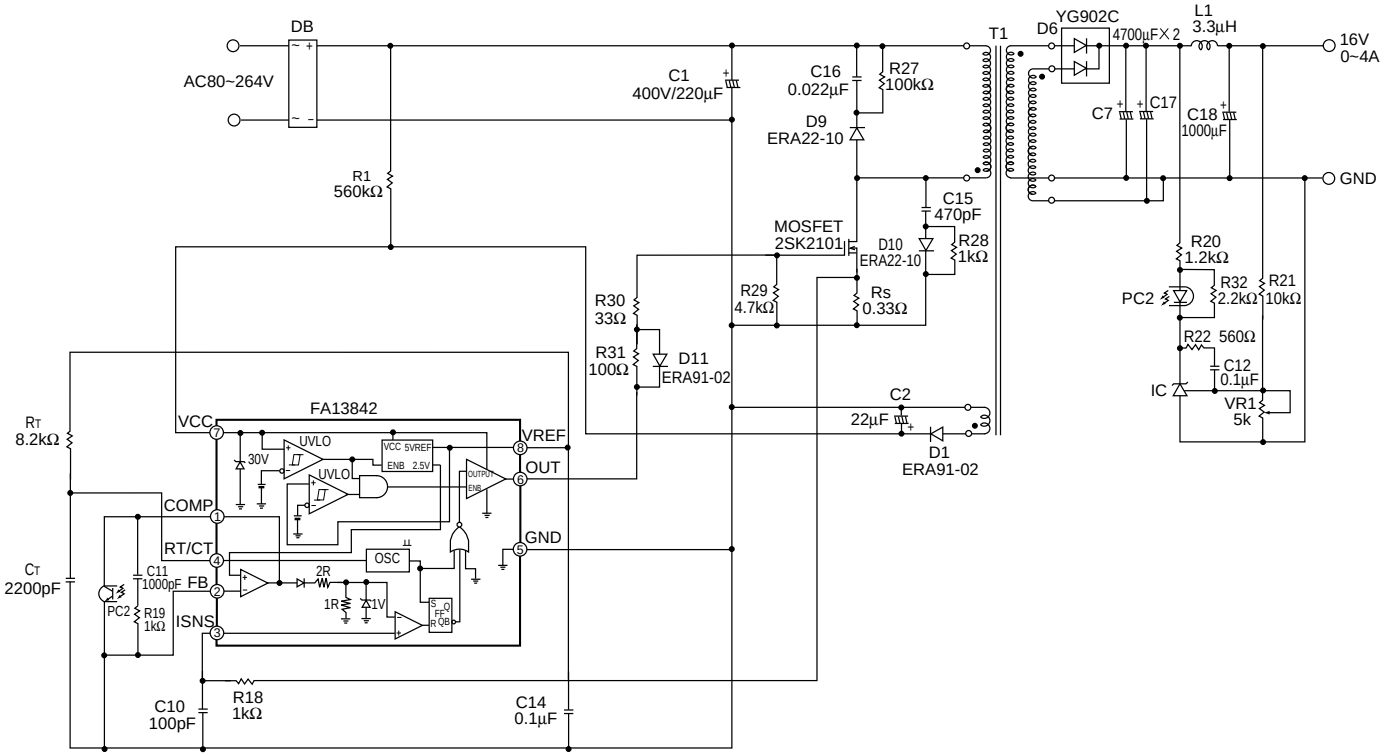


Fig. 25

■ Application circuit



Parts tolerances characteristics are not defined in the circuit design sample shown above. When designing an actual circuit for a product, you must determine parts tolerances and characteristics for safe and economical operation.